

CHIST-ERA Conference 2011, 5th-6th September, Cork

Nanotechnology Designed for Energy-Sustainable Electronics



***“from...
atoms
to...
systems”***

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Electronics Theory Group
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Nanotechnology Designed for Energy-Sustainable Electronics Agenda

the Grand challenge (or... why are we here?)

- Energy consumption on the rise
- Consumer electronics

opportunities for ICT (or... what can we do?)

- Low-power (autonomous) devices (More-Moore)
- Devices for energy efficiency (More-than-Moore)

a nano-inspired bottom-up approach (or... why nanotechnology?)

- From atoms to materials to devices
- more Moore: ideal sub-threshold slopes at the nanoscale
- more than Moore: nanomaterials for energy harvesting

expected impact (or... what are the outputs?)



Nanotechnology Designed for Energy-Sustainable Electronics

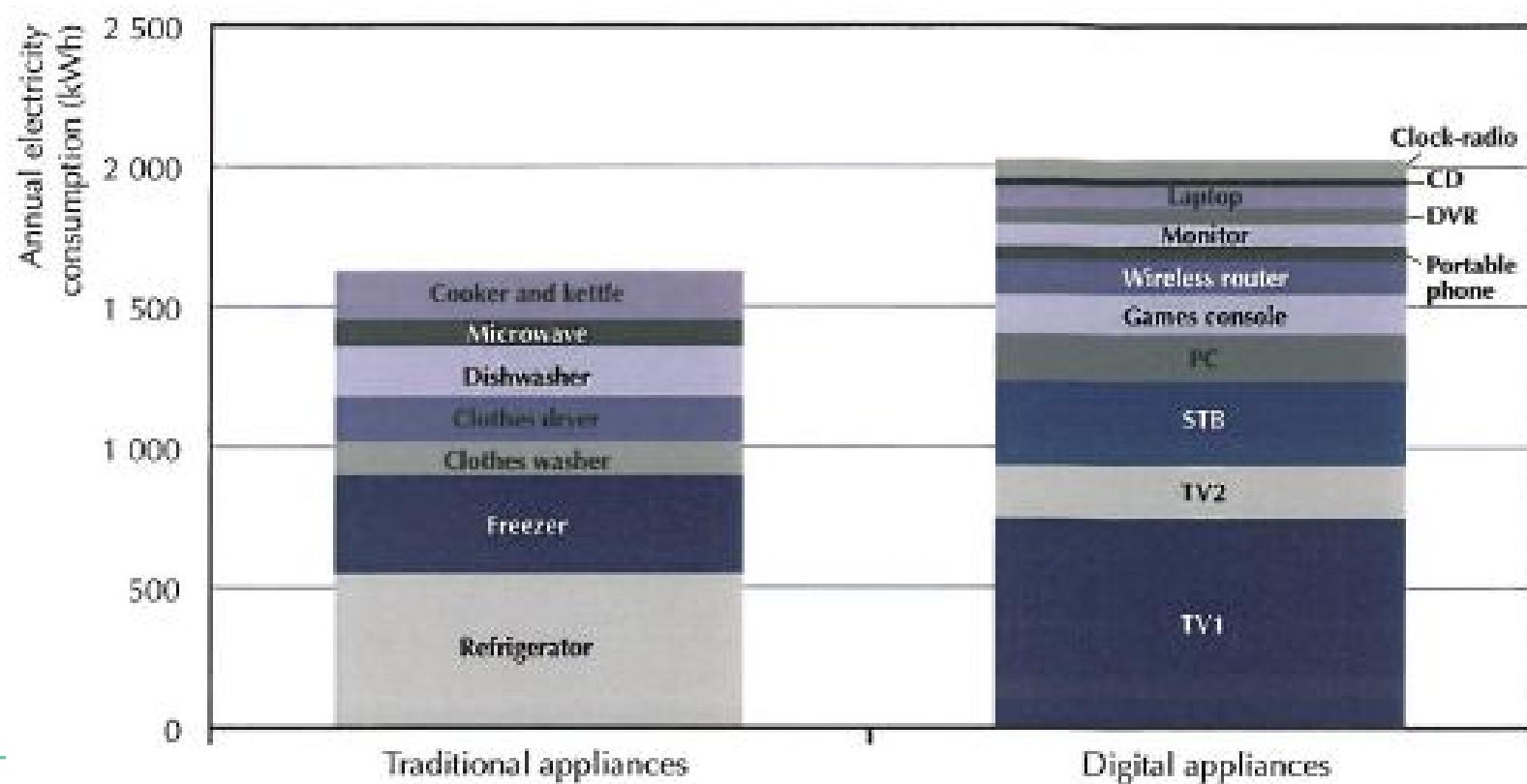
the Grand challenge
opportunities for ICT
a nano-inspired bottom-up approach
expected impact





ICT energy pie grows fast!

ICT and consumer electronics account for approximately 15% of global residential electricity consumption



Data: IEA report (2009)



1,700 TWh in two decades!

By 2030, energy use by household ICT and consumer electronics will triple consuming 1,700TWh

4,344 TWh



3,457 TWh



1,038 TWh



Maps: <http://en.wikipedia.org>
Data: IEA report (2010)

www.tyndall.ie

Nanotechnology Designed for Energy-Sustainable Electronics

the Grand challenge
opportunities for ICT

a nano-inspired bottom-up approach

➤ Co-design of nanotechnology-enhanced ICT
expected impact

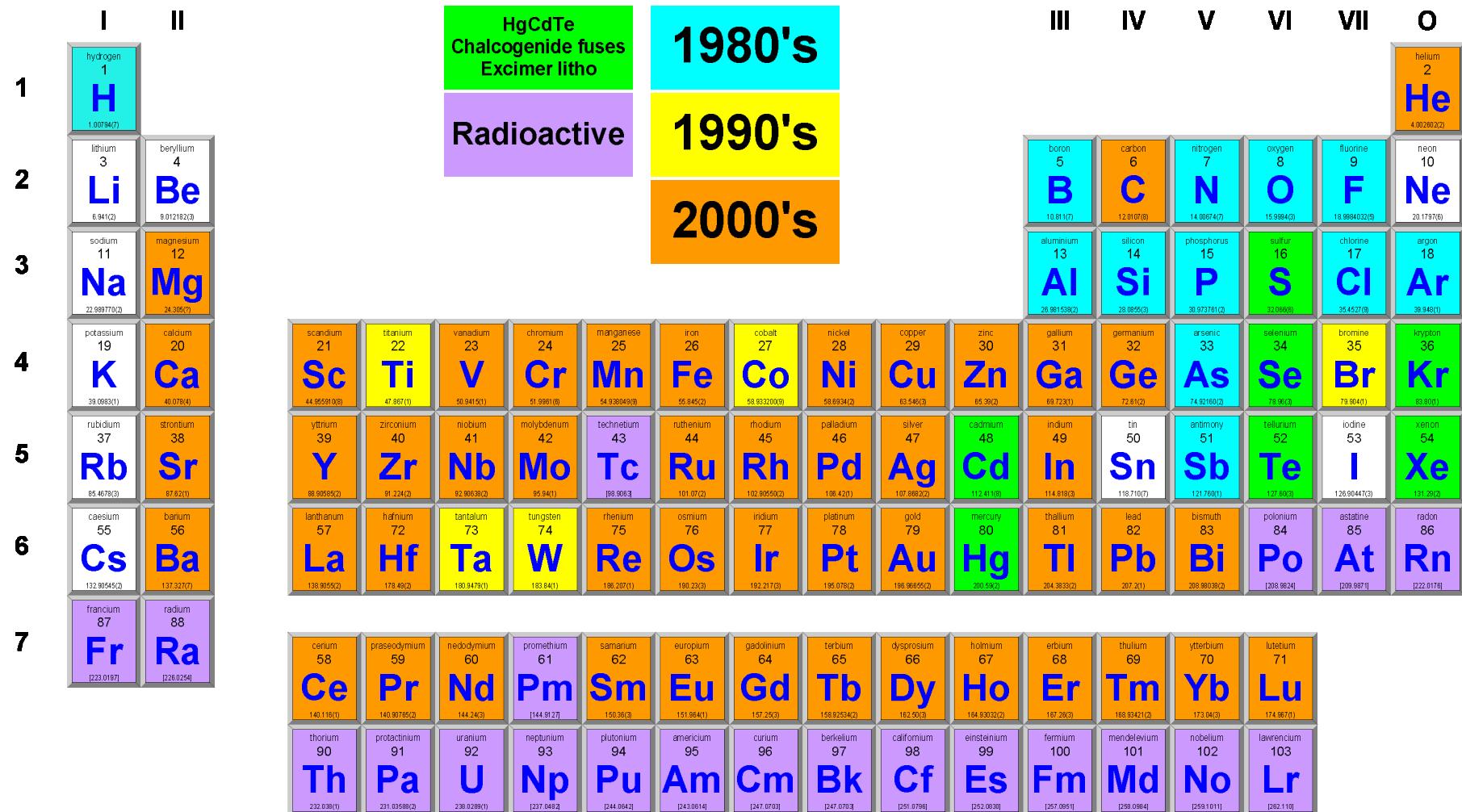




Technology Booster 1

Elements used in Chip Fabrication

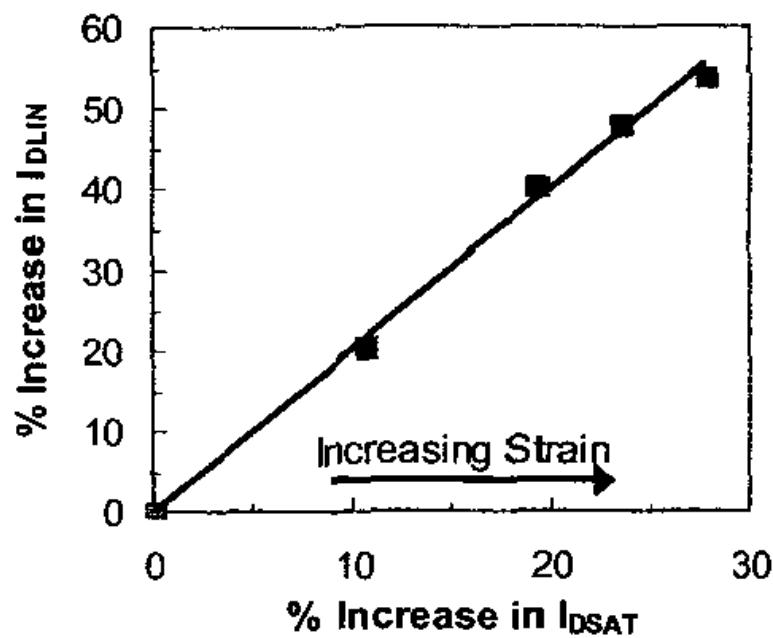
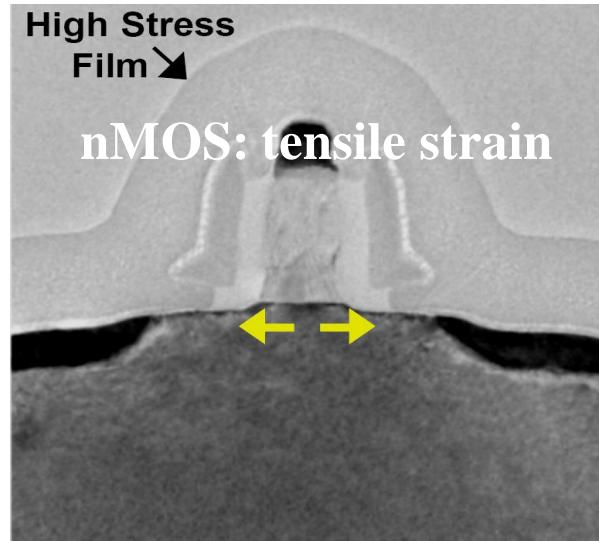
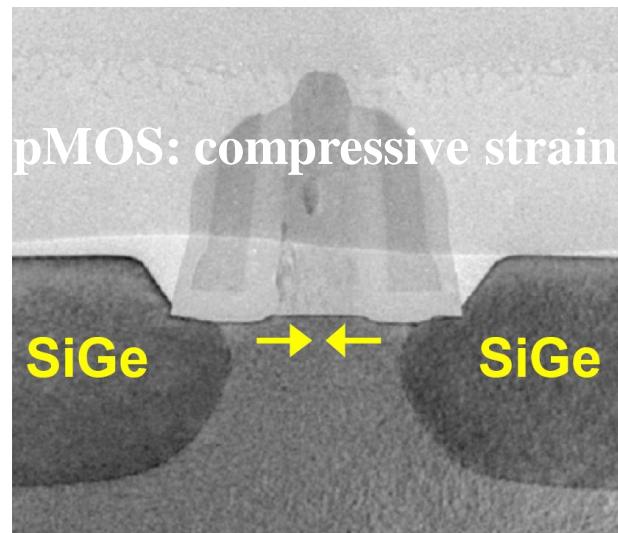
Courtesy J.-P. Colinge





Technology Booster 2

Mobility enhancement by strain



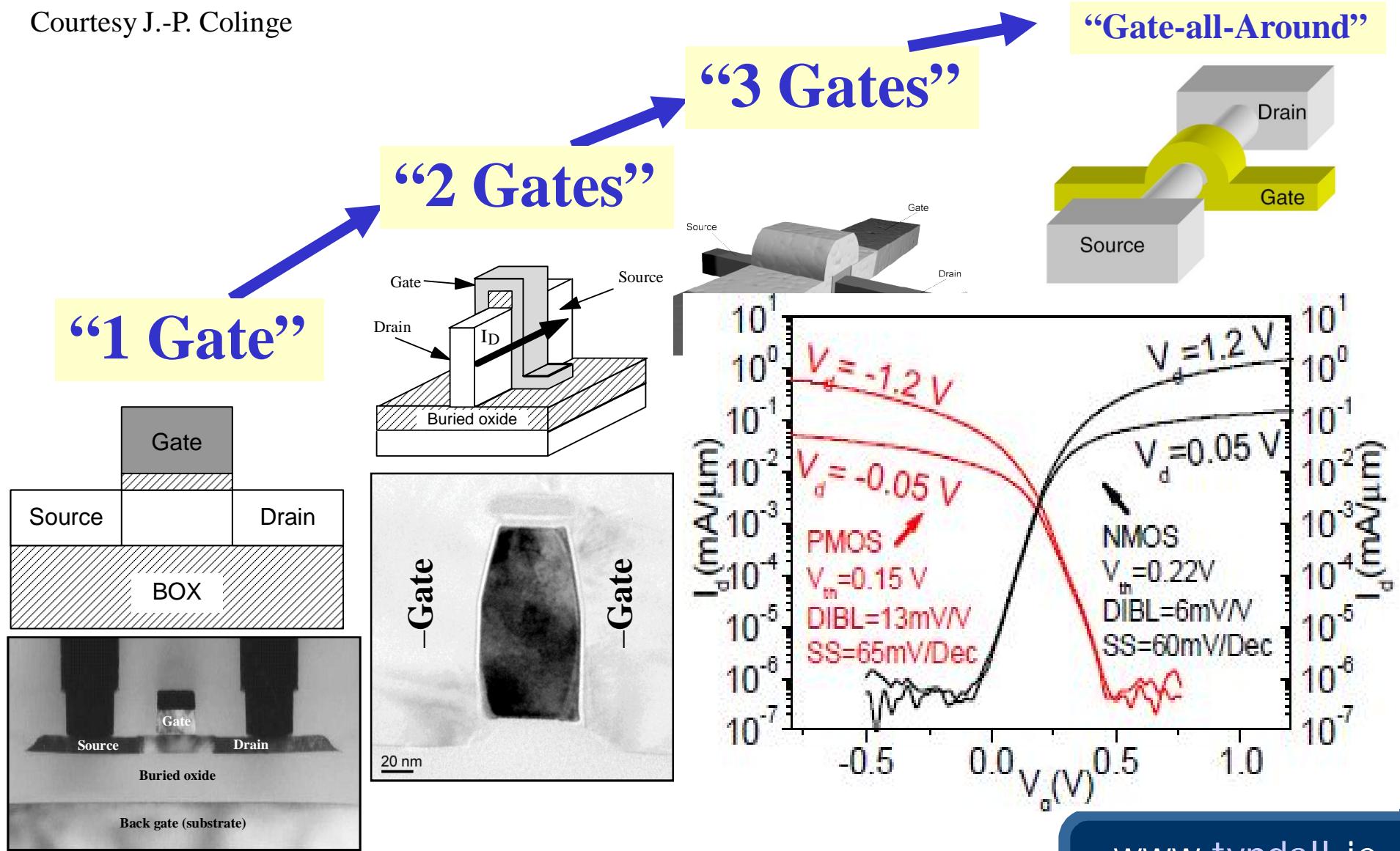
A 90nm High Volume Manufacturing Logic Technology
Featuring Novel 45nm Gate Length Strained Silicon
CMOS Transistors
T. Ghani et al, IEDM 2003, p. 978



Technology Booster 3

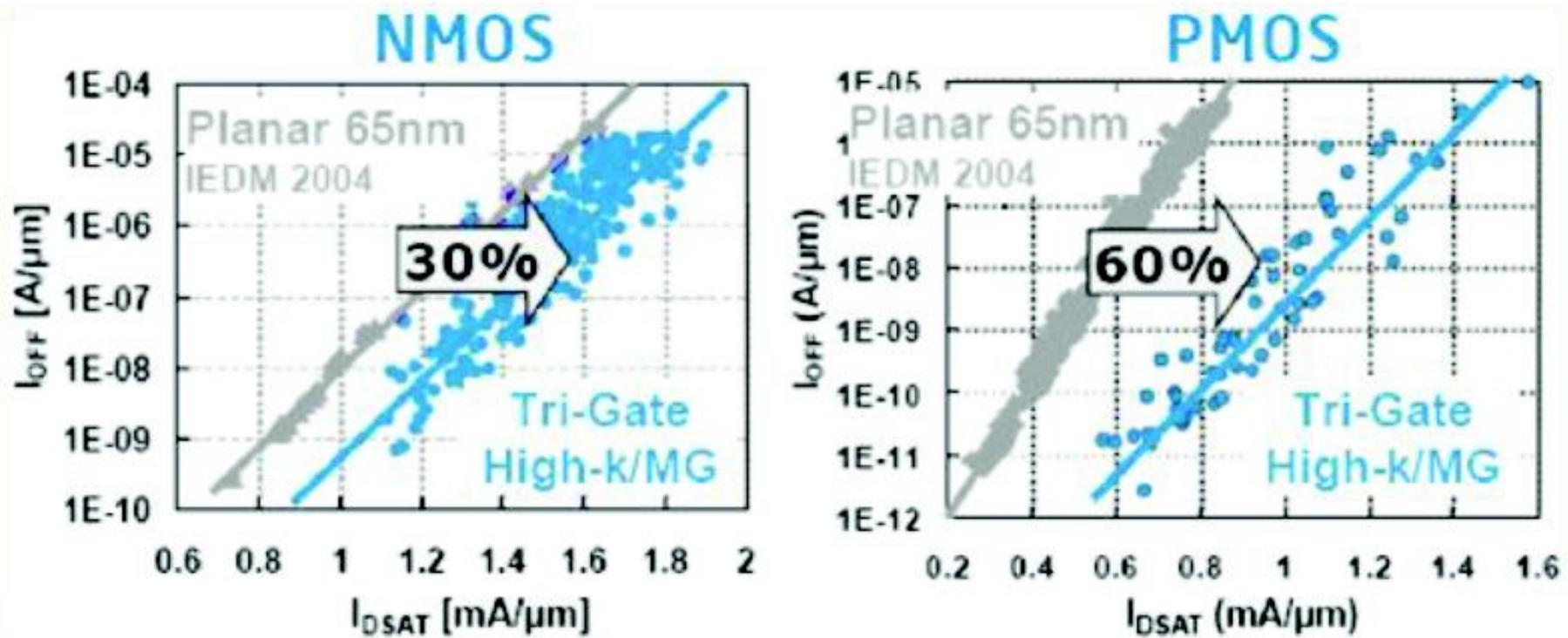
Evolution of Transistors Geometry

Courtesy J.-P. Colinge





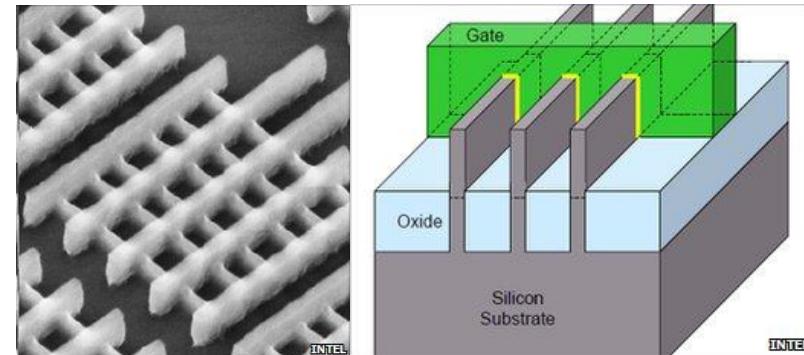
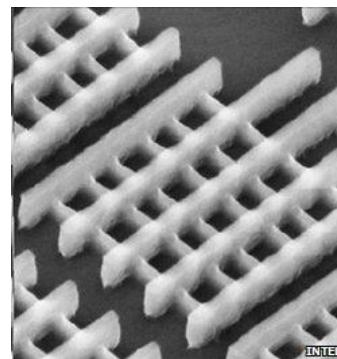
Transistor scaling why nanowires?



R. S. Chau,
Technology@Intel Magazine (2006)



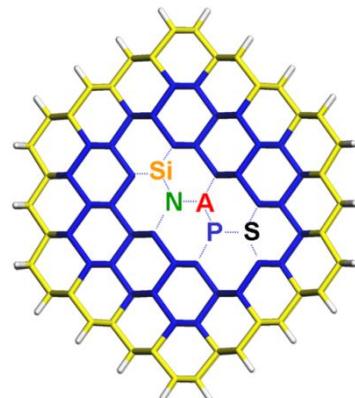
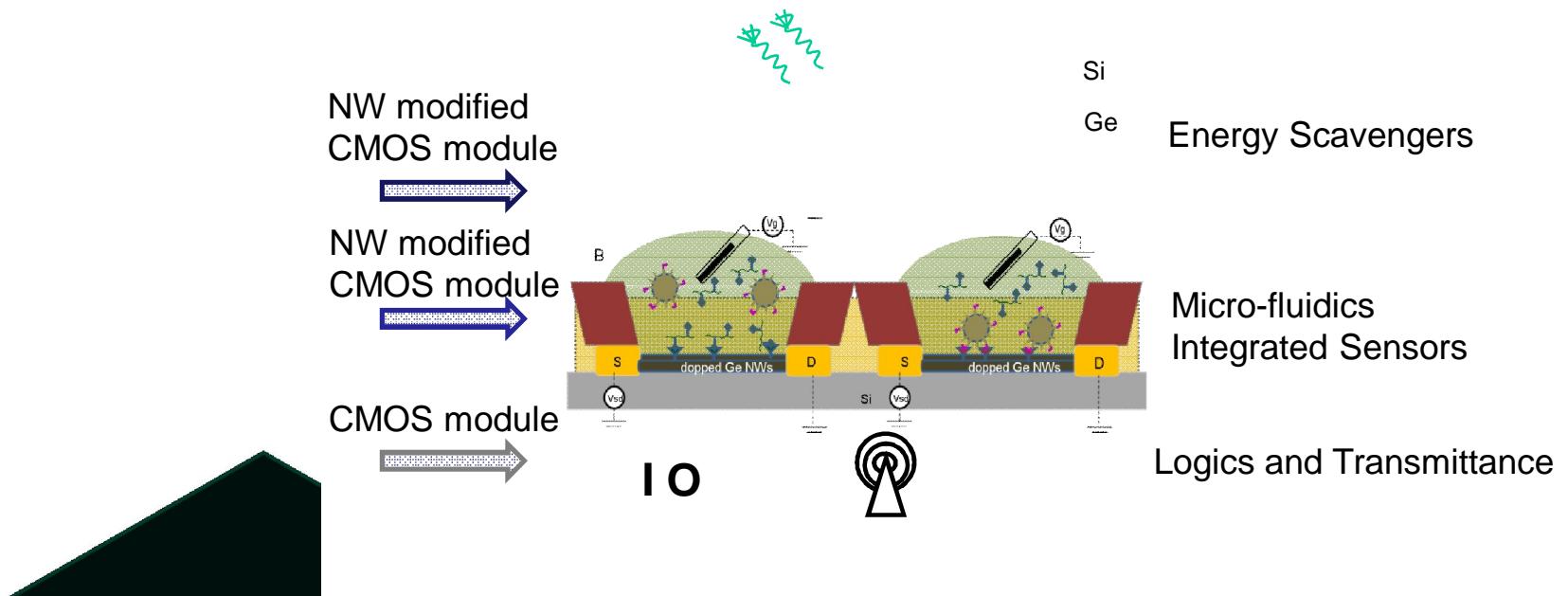
Intel 22nm Ivy Bridge (2011)





Semiconducting Nanowire Platform for Autonomous Sensors SiNAPS

SiNAPS mote concept (see www.sinaps-fet.eu)



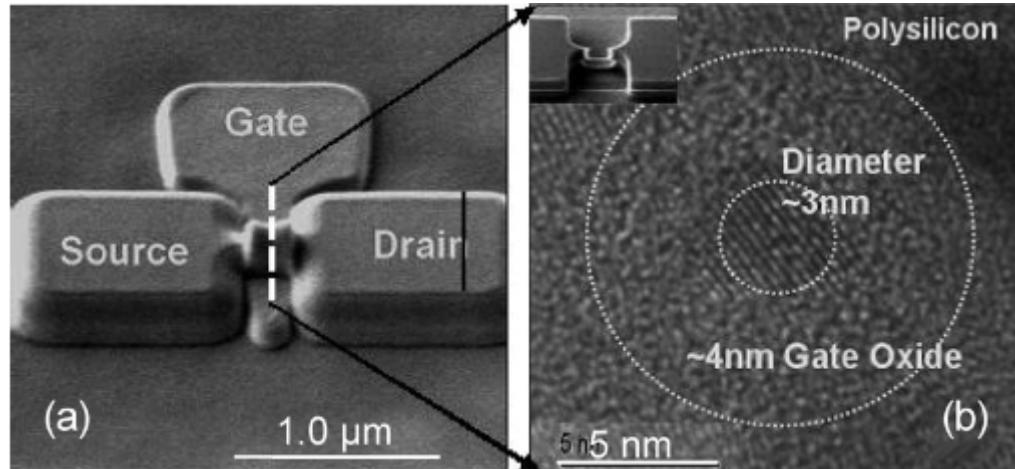
Imperial College
London



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Nanoelectronics meets atomic design

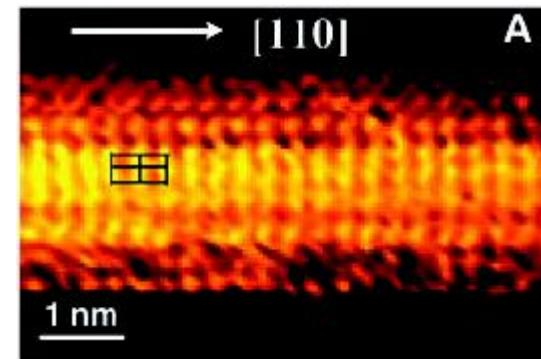


Top-down

Sing *et al*, IEEE TED **55**, 3107 (2008)

Bottom-up

Ma *et al*, Science **299**, 1876 (2003)



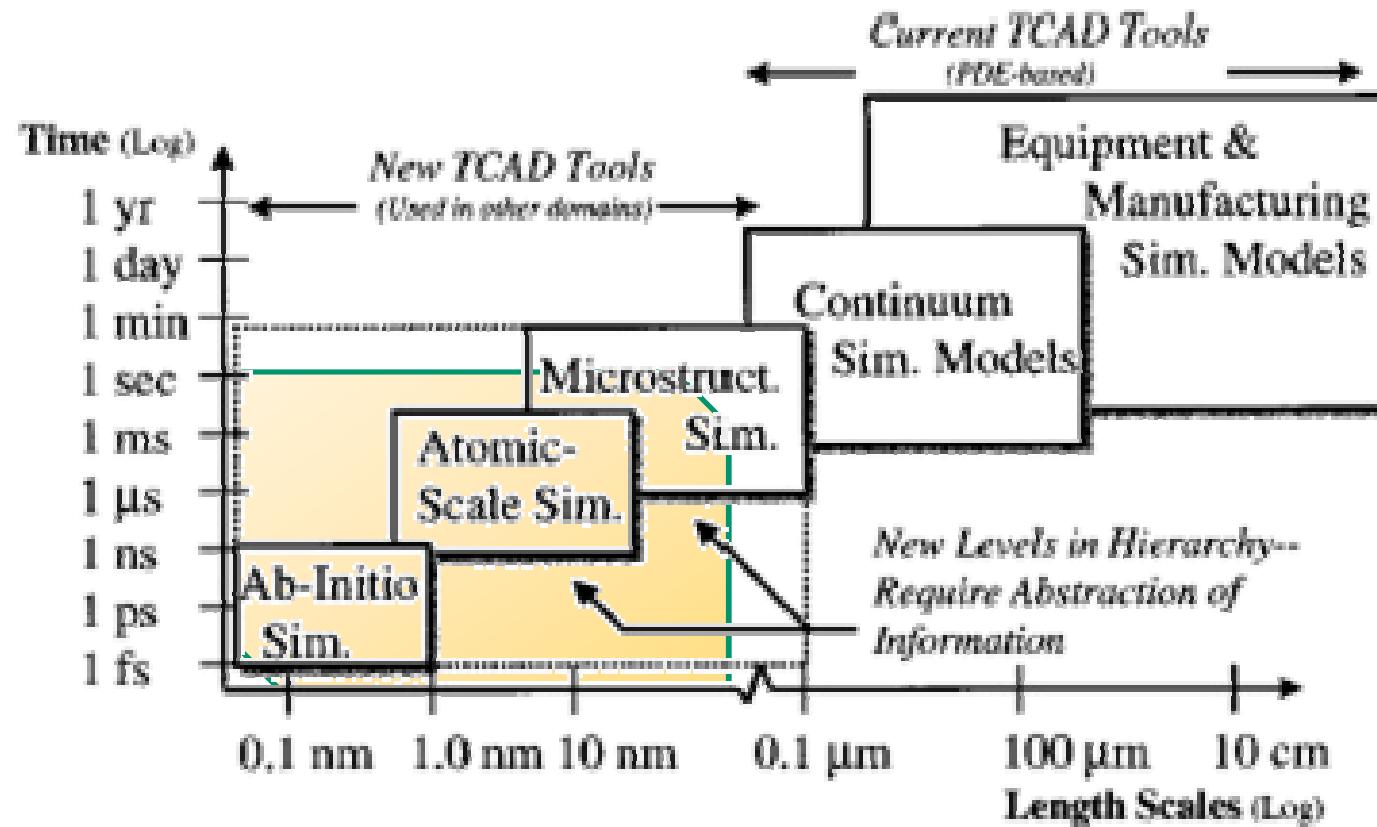
size convergence with atomic-scale modelling



www.tyndall.ie



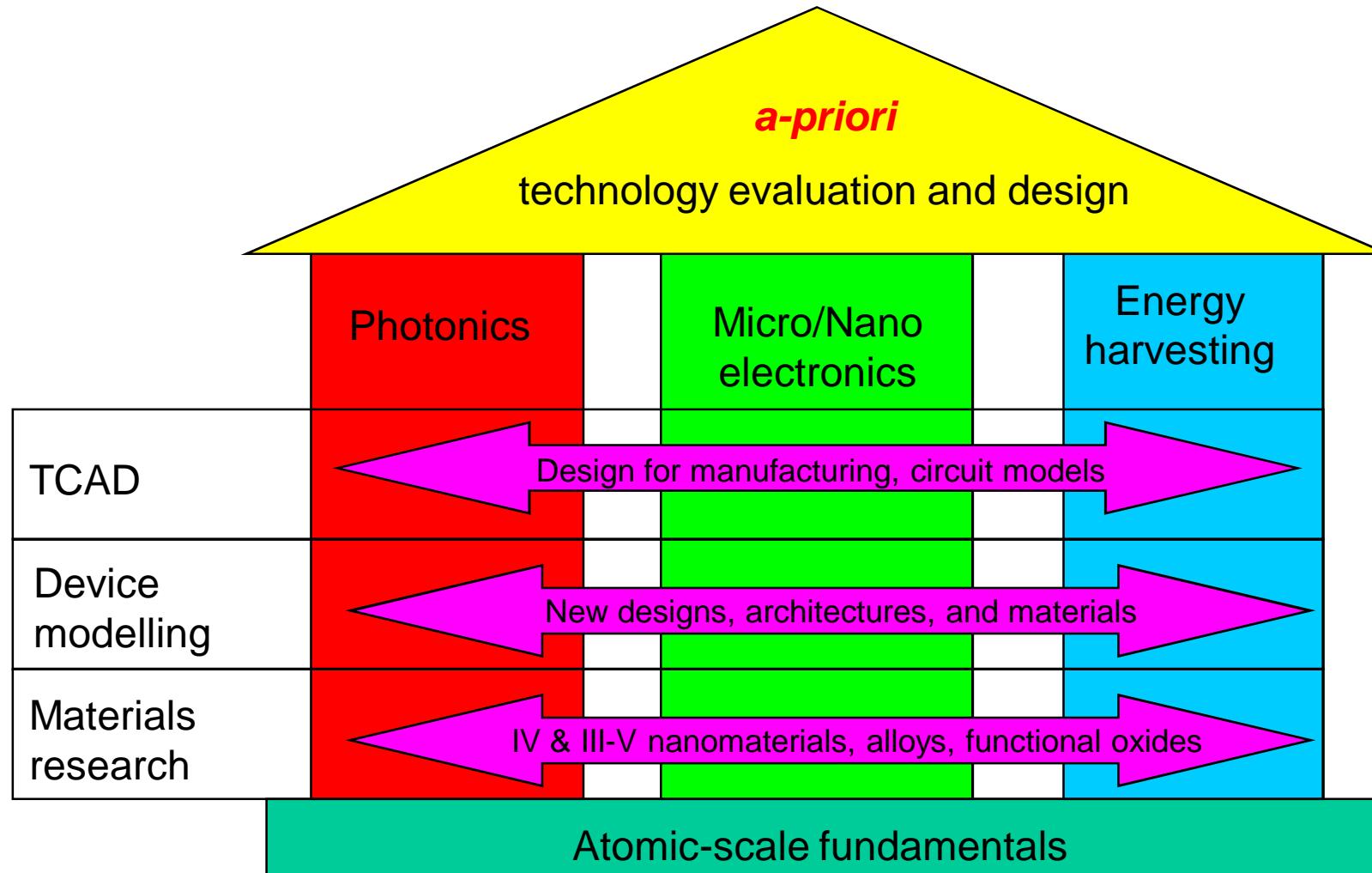
TCAD tools hierarchy



R.W. Dutton and A.J Strojwas, IEEE Trans. CAD of ICS 19, 1544 (2000)



Co-design of nanotechnology-enhanced ICT



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- Example 1: ideal sub-threshold slopes at the nanoscale

expected impact

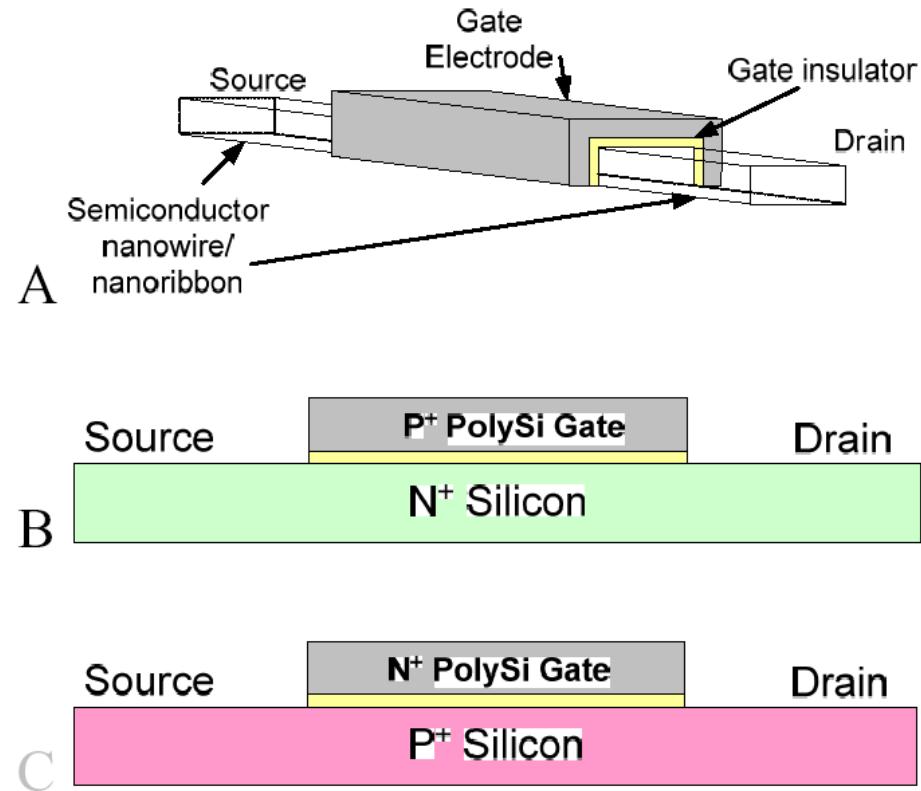
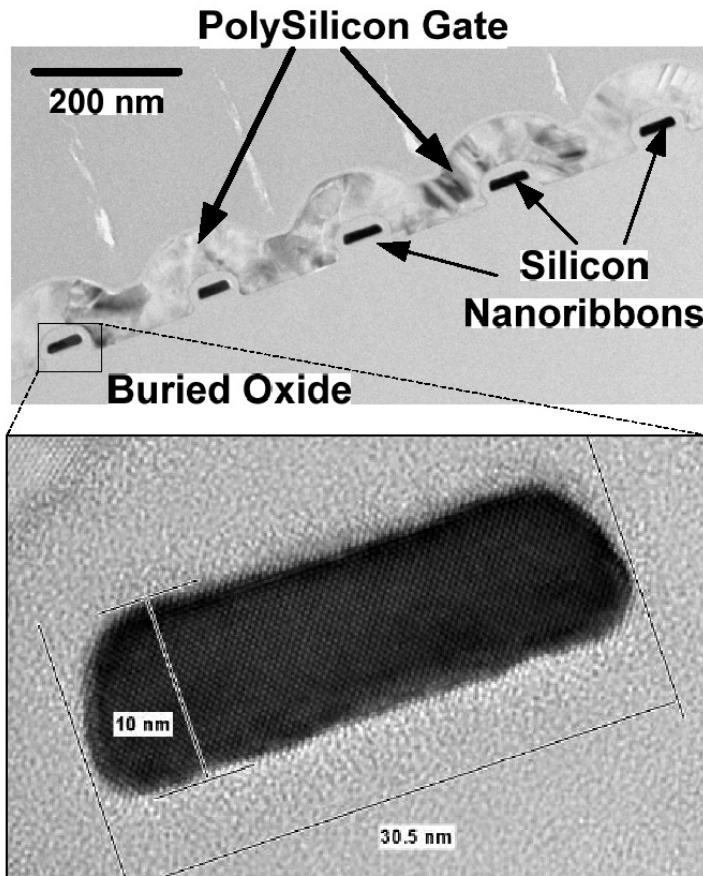




Junctionless transistor

Gated Resistor (or CMOS without junctions) → no doping gradients

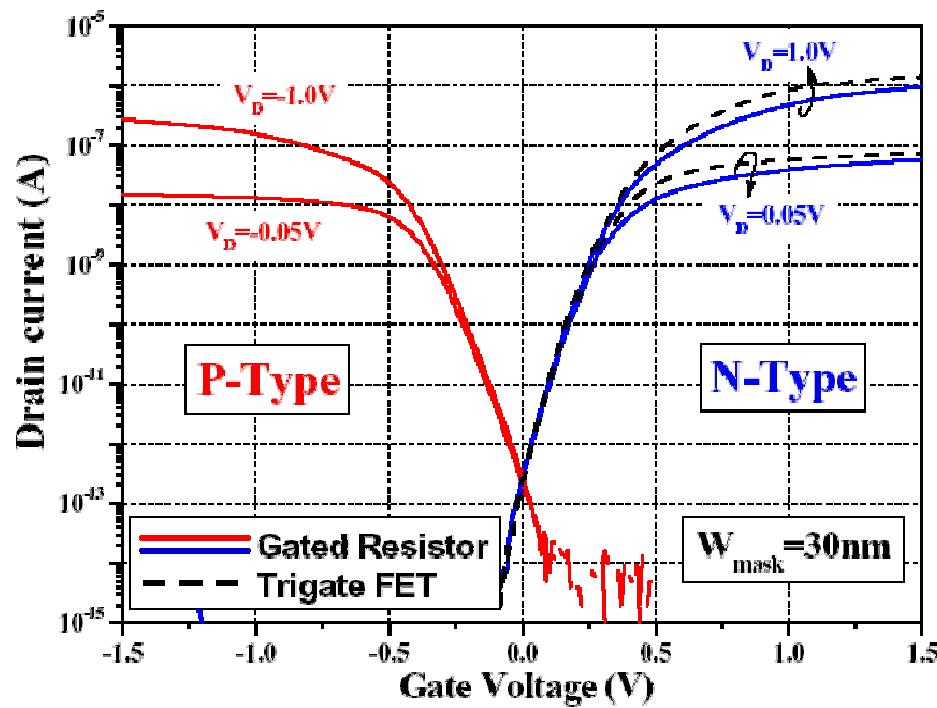
The cross-section of the channel is small enough that gate can deplete the heavily doped channel ($8 \times 10^{19} \text{ cm}^{-3}$) entirely, hence can turn off device



J.-P. Colinge et al, Nat. Nanotech. 5, 225 (2010)

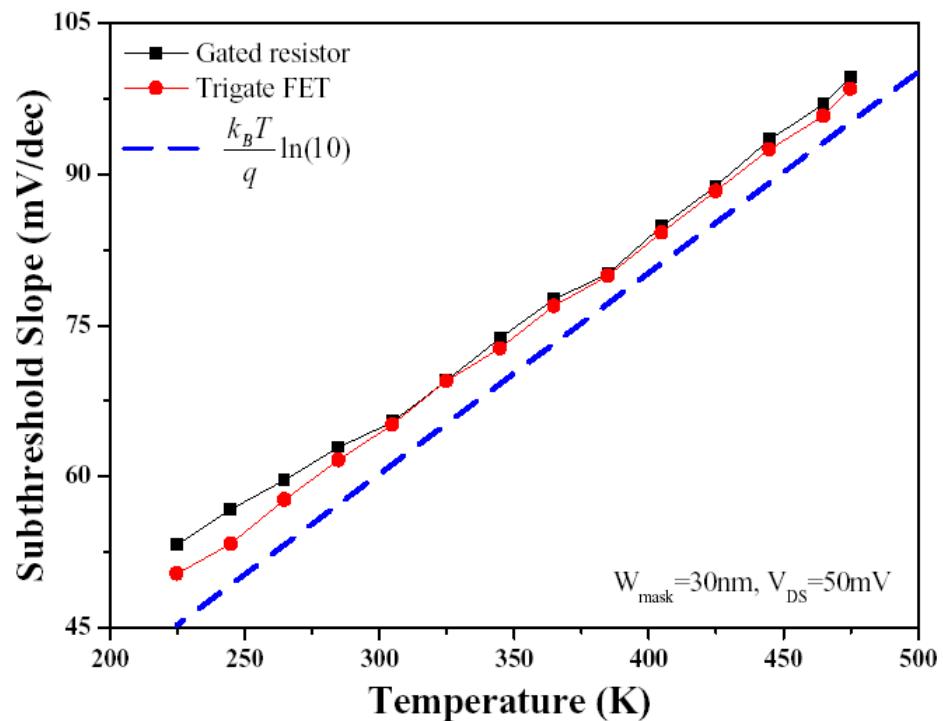


Junctionless transistor characteristics



J.-P. Colinge et al, Nat. Nanotech. **5**, 225 (2010)

$$SS = \frac{dV_G}{d \log(I_D)}$$

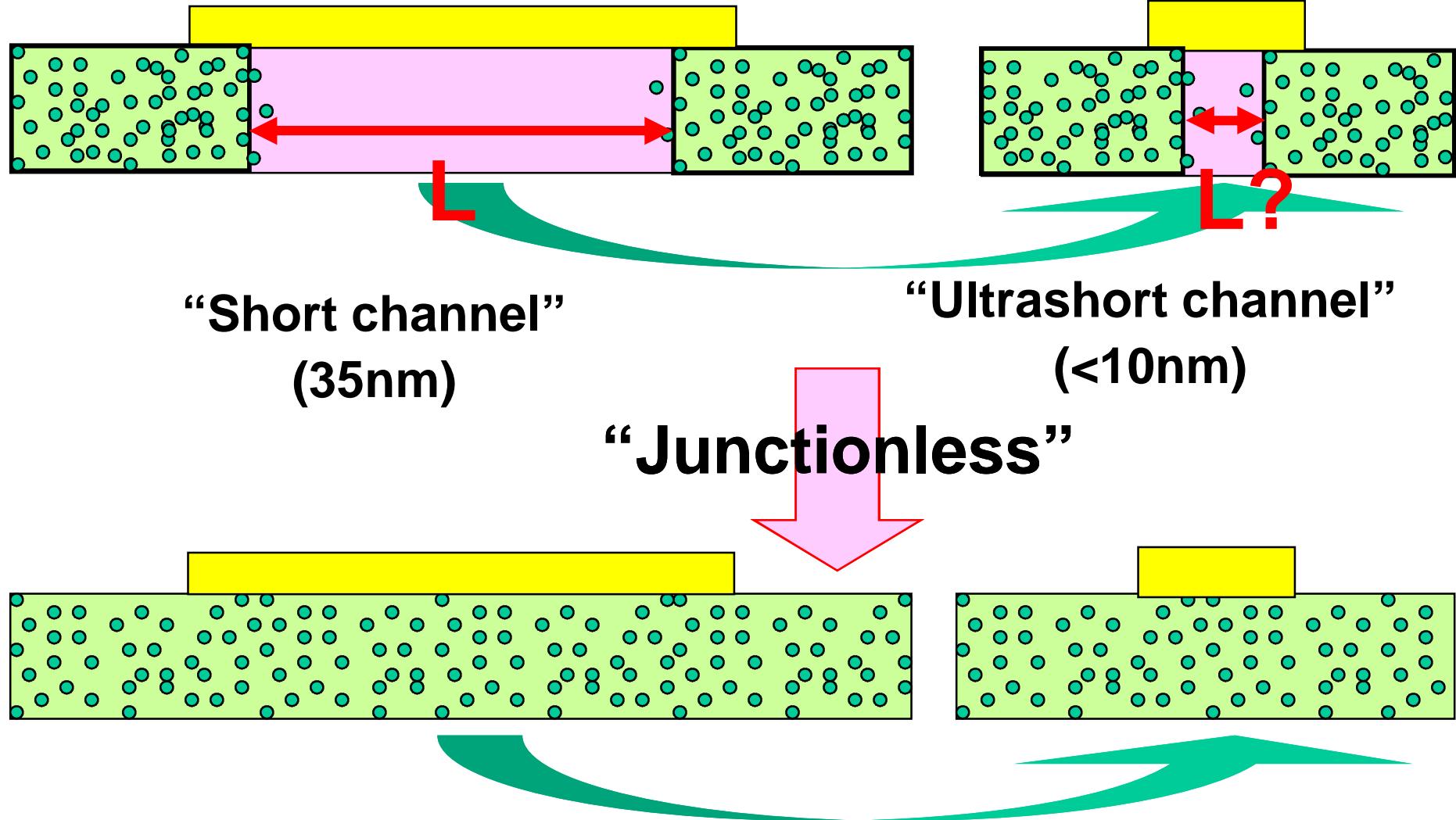


new devices show even smaller short channel effects



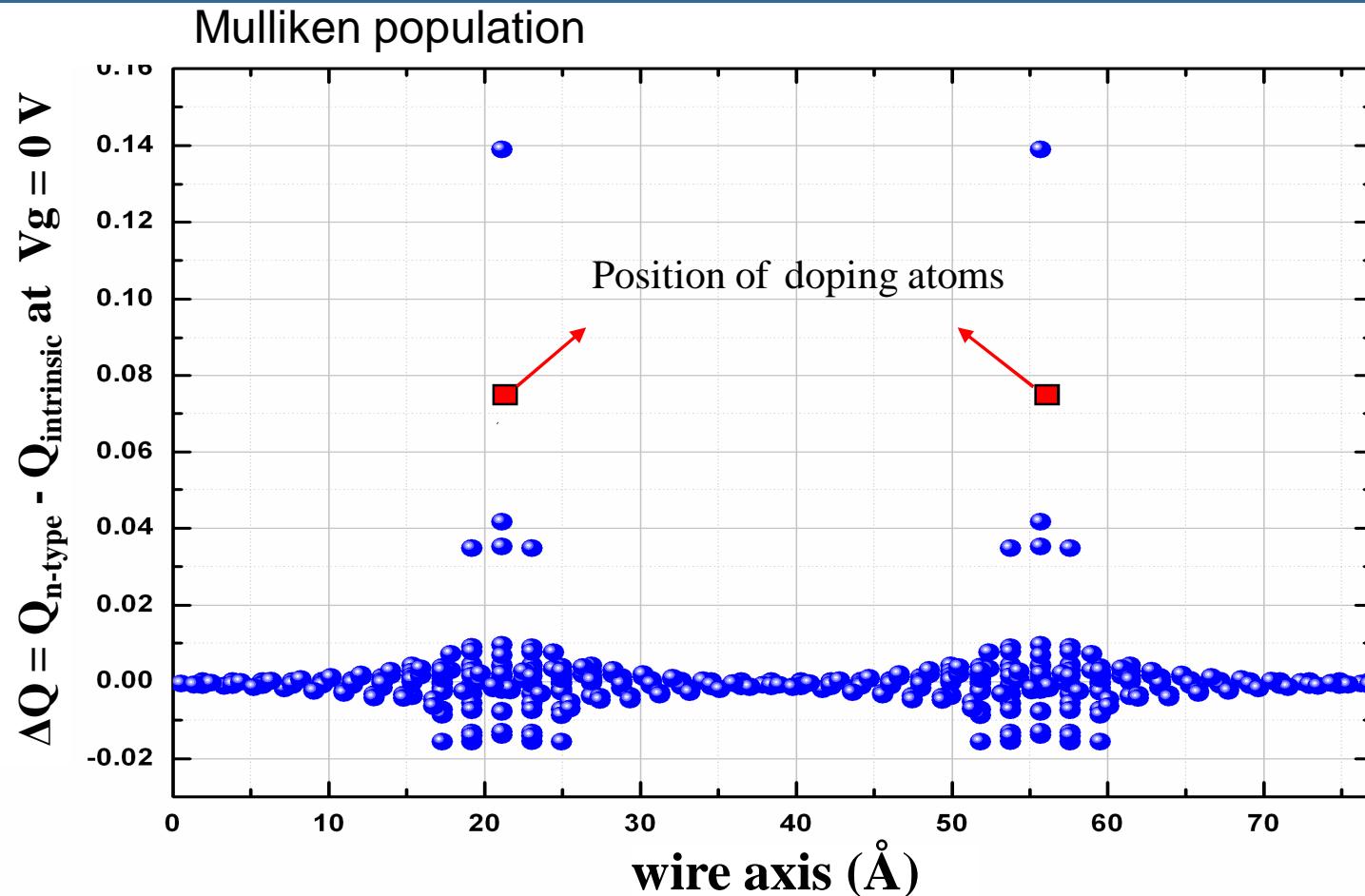


Dopant profile issue





Dopants in nanowires fundamental limitation for junctions



localization radius of the dopant electron or hole is $\sim 1.5 \text{ nm}$

L. Ansari, B. Feldman, G. Fagas, J.-P. Colinge, and J. C. Greer,
Appl. Phys. Lett. **97**, 062105 (2010)



(Junctionless) transistor scaling

- Classical device simulation

C.W. Lee *et al*, Appl. Phys. Lett. **94**, 053511 (2009)

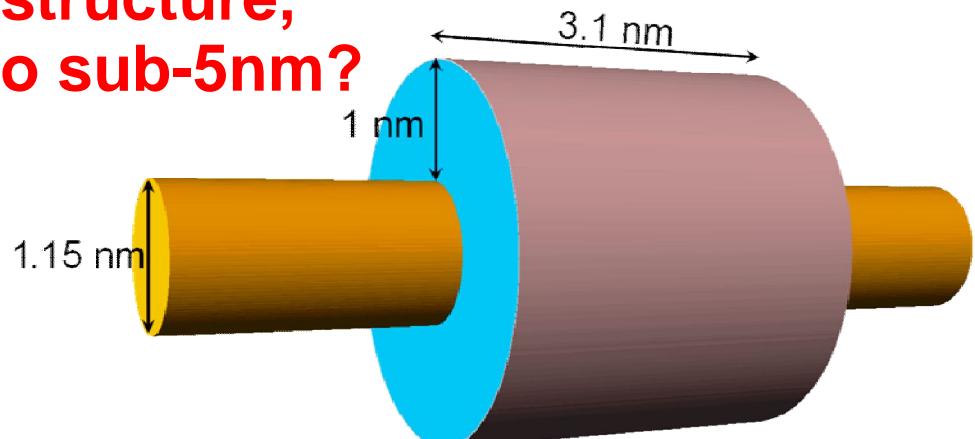
- Experimental device

J.-P. Colinge *et al*, Nature Nanotech. **5**, 225 (2010)

- Geometry dependence in classical and quantum devices

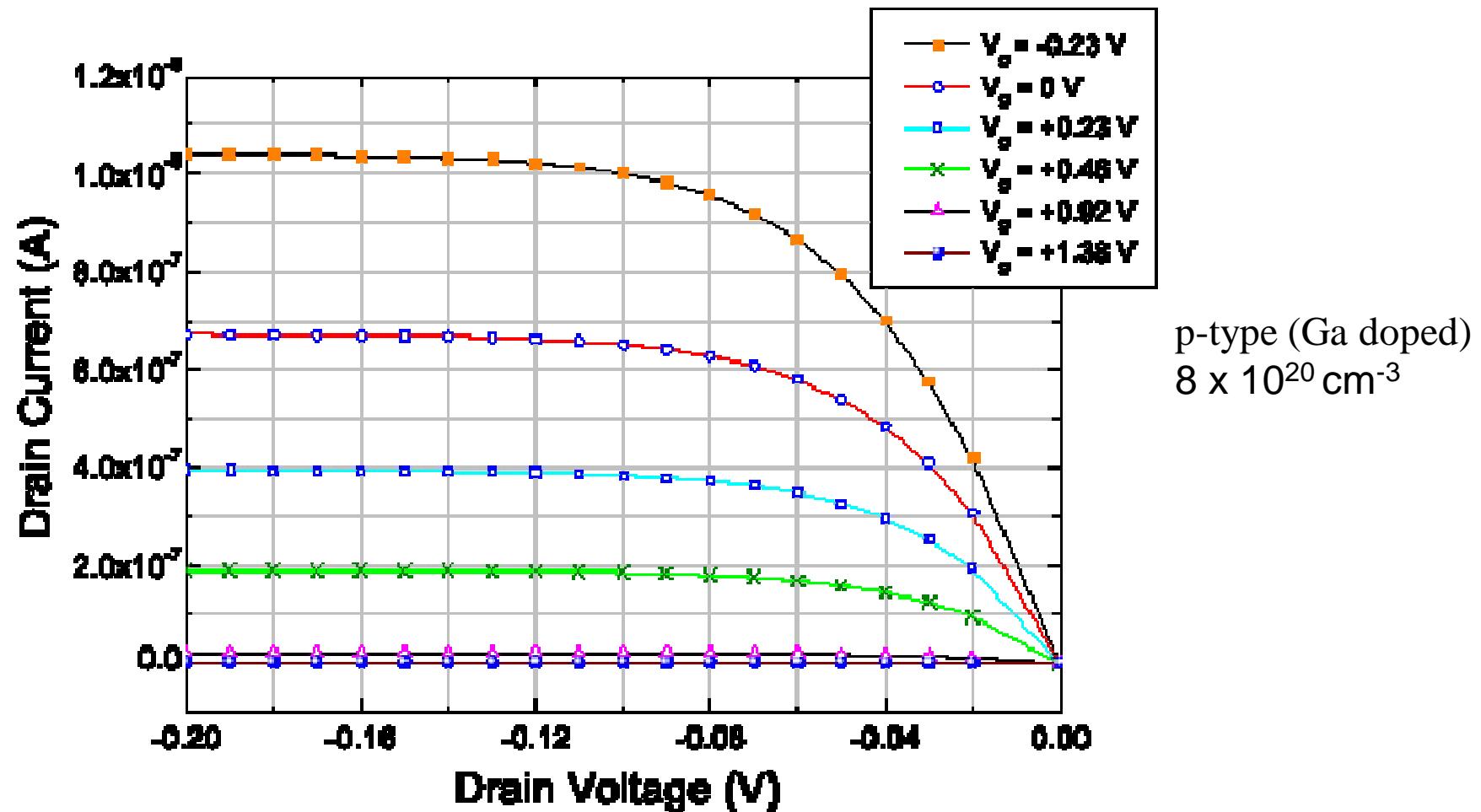
P. Razavi *et al*, submitted (2011)

**Using realistic electronic structure,
can the device scale down to sub-5nm?**





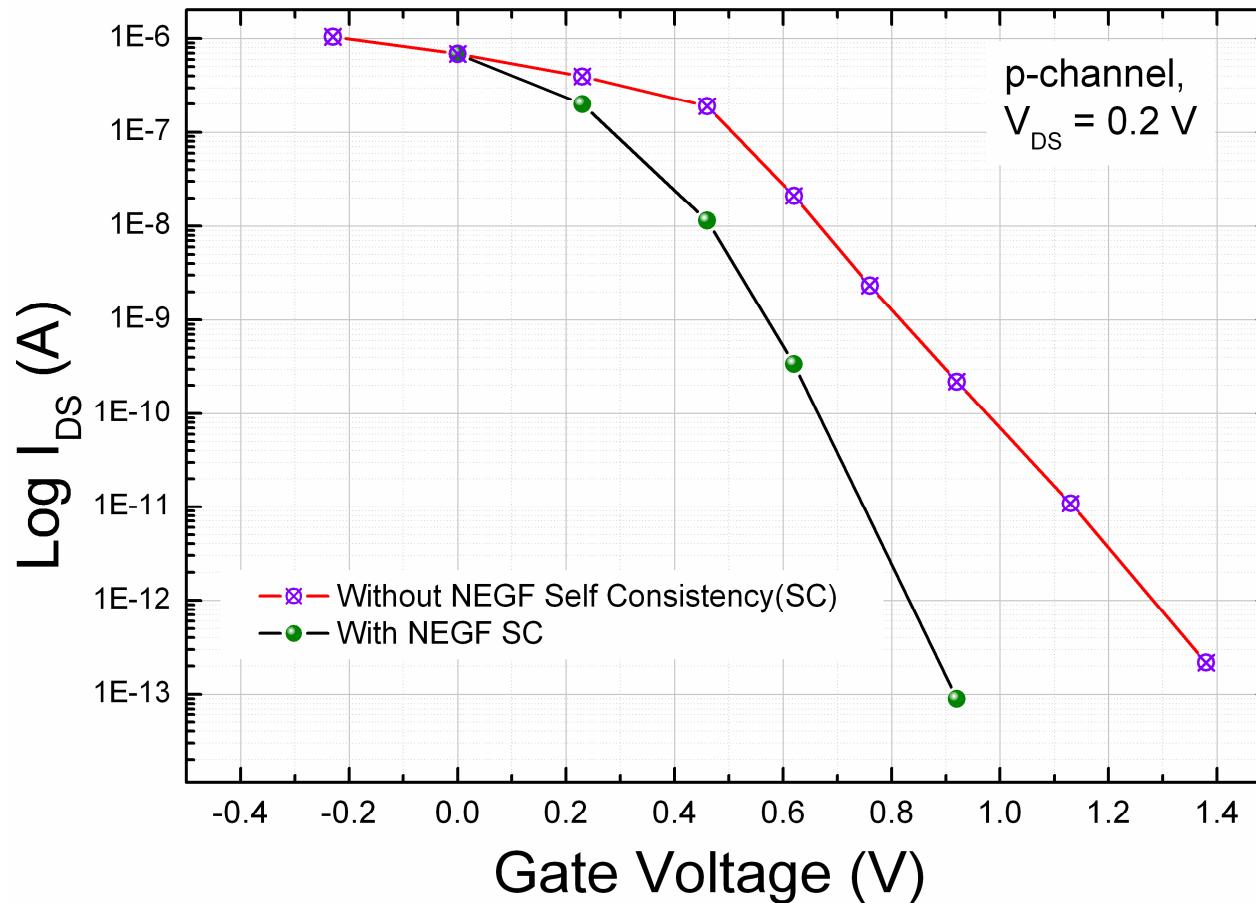
Transistor behaviour at 3nm



L. Ansari, B. Feldman, G. Fagas, J.-P. Colinge, and J. C. Greer,
Appl. Phys. Lett. **97**, 062105 (2010)



Subthreshold slope

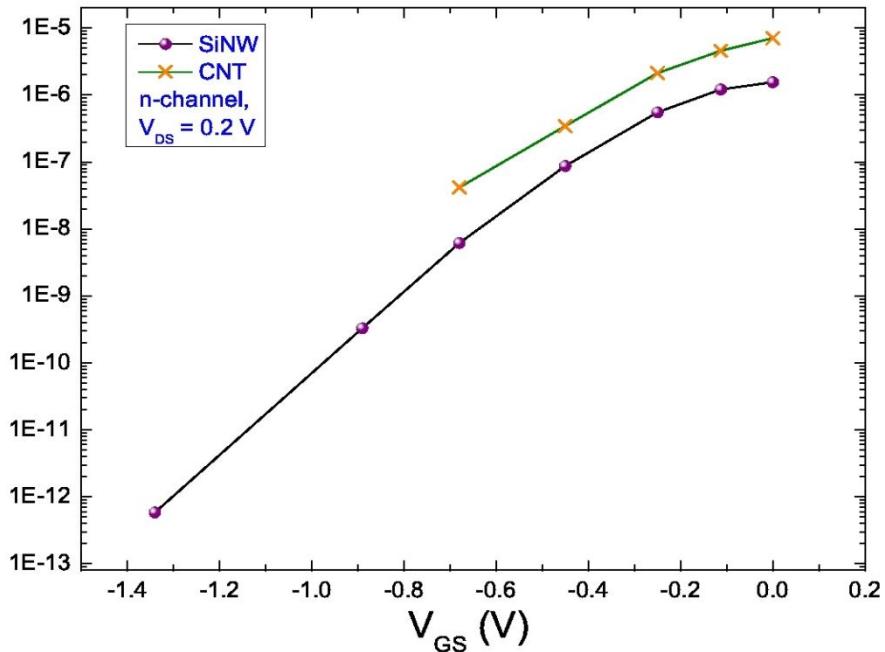
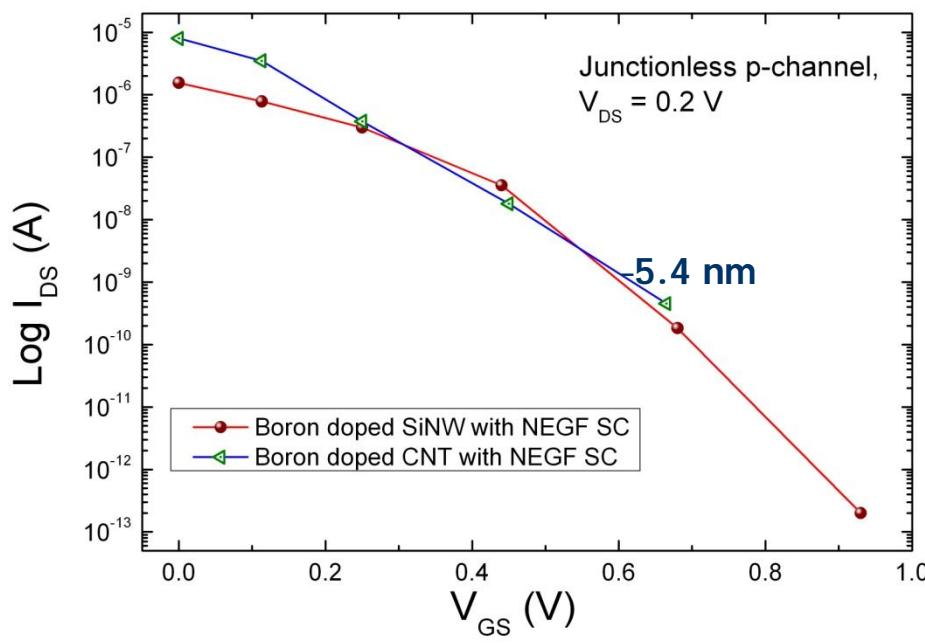
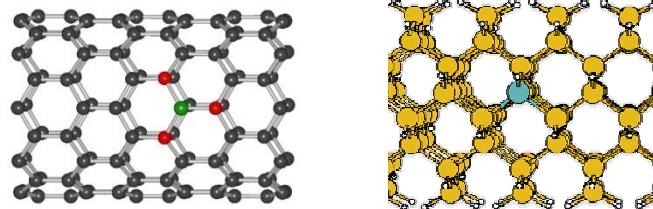


~ 80 mV /decade → near to theoretical limit!

L. Ansari, B. Feldman, G. Fagas, J.-P. Colinge, and J. C. Greer,
Sol. Stat. Elec. (2011)



Si and CNT JL transistors comparison



L. Ansari et al, in preparation

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➤ Example 2: nanomaterials for energy harvesting
expected impact





Energy harvesting possibilities

Battery
operated
systems



Ambient energy

R. J. M. Vullers, Zero-Power ICT Workshop 2009
R. J. M. Vullers *et al*, Solid-State Elec.**53**, 684 (2009)

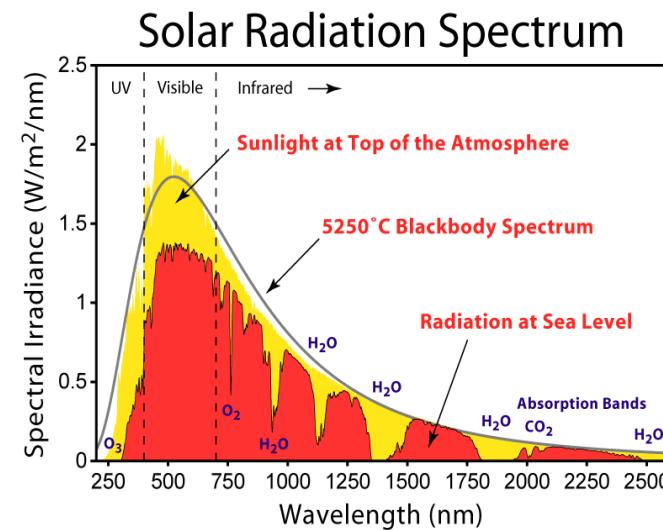
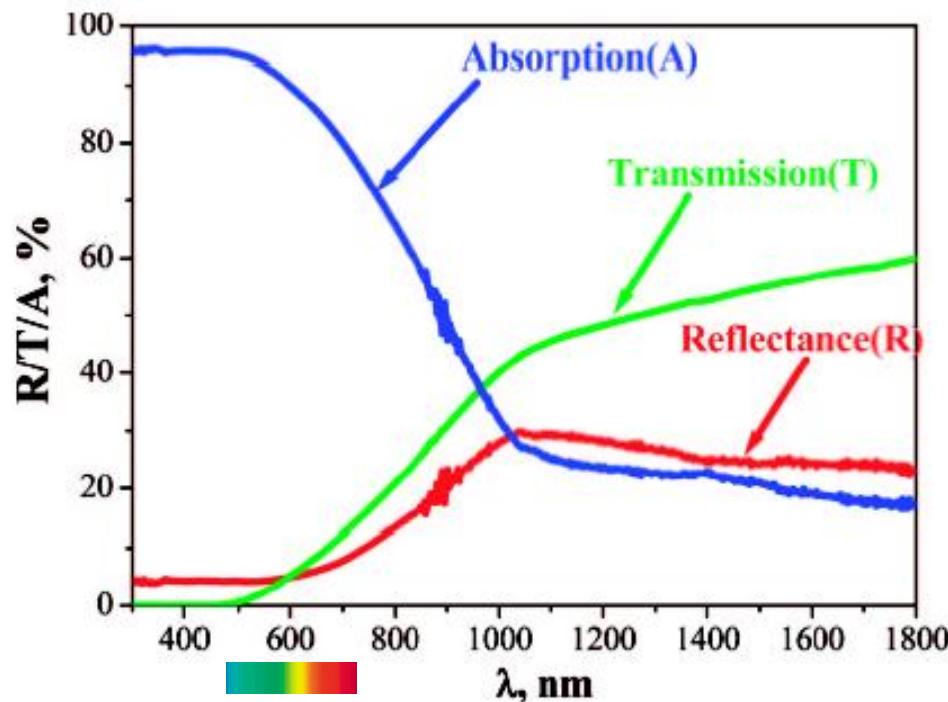
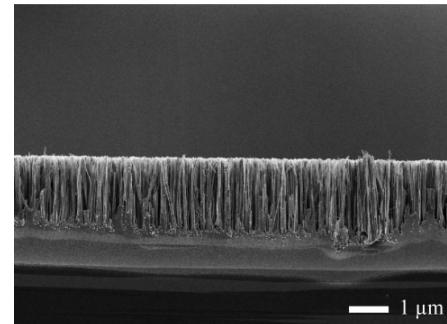
Source	Source power	Harvested power
Ambient light		
Indoor	0.1 mW/cm ²	10 µW/cm ²
Outdoor	100 mW/cm ²	10 mW/cm ²
Vibration/motion		
Human	0.5 m @ 1 Hz 1 m/s ² @ 50 Hz	4 µW/cm ²
Industrial	1 m @ 5 Hz 10 m/s ² @ 1 kHz	100 µW/cm ²
Thermal energy		
Human	20 mW/cm ²	30 µW/cm ²
Industrial	100 mW/cm ²	1–10 mW/cm ²
RF		
Cell phone	0.3 µW/cm ²	0.1 µW/cm ²



Axial junctions in nanowire arrays



antireflection effect in NW arrays
up to 4.4% efficiency under 1-sun illumination

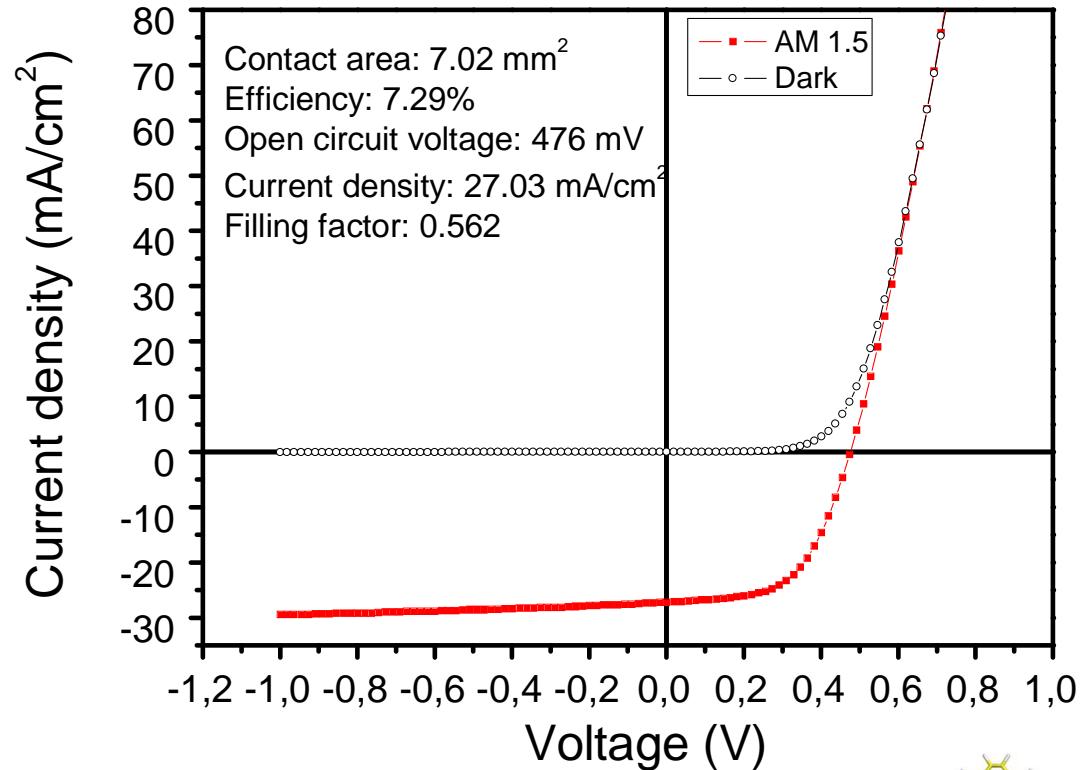
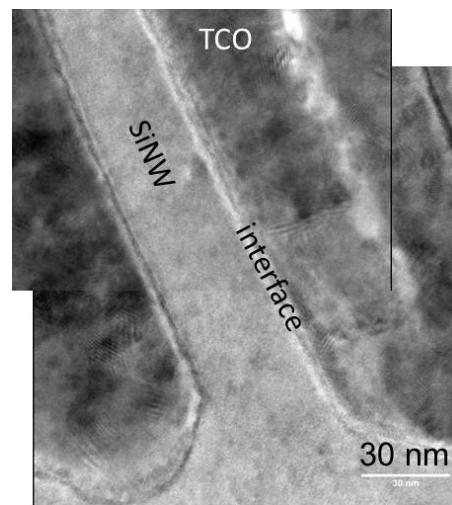
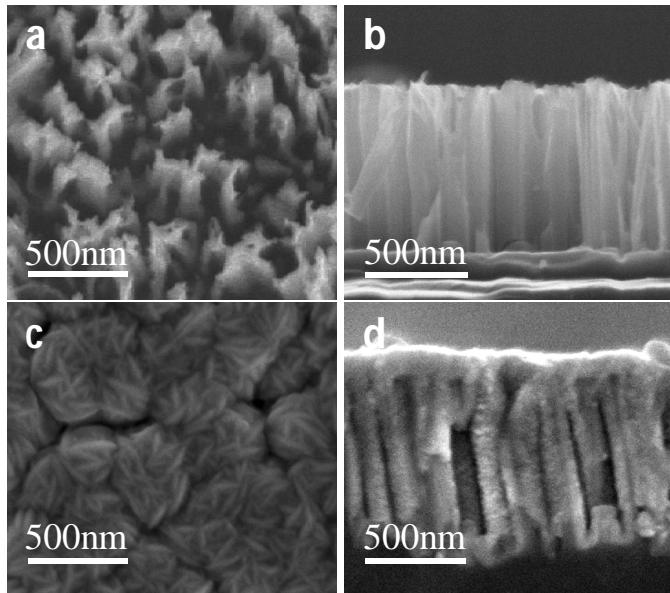


<http://en.wikipedia.org>

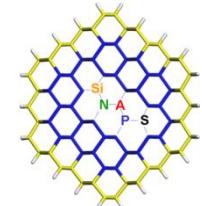
V. Sivakov, G. Andrä, A. Gawlik, A. Berger, J. Plenz, F. Falk, S.H. Christiansen, Nano Lett. **9**, 1549 (2009)



Arrays of nanowire coaxial cables



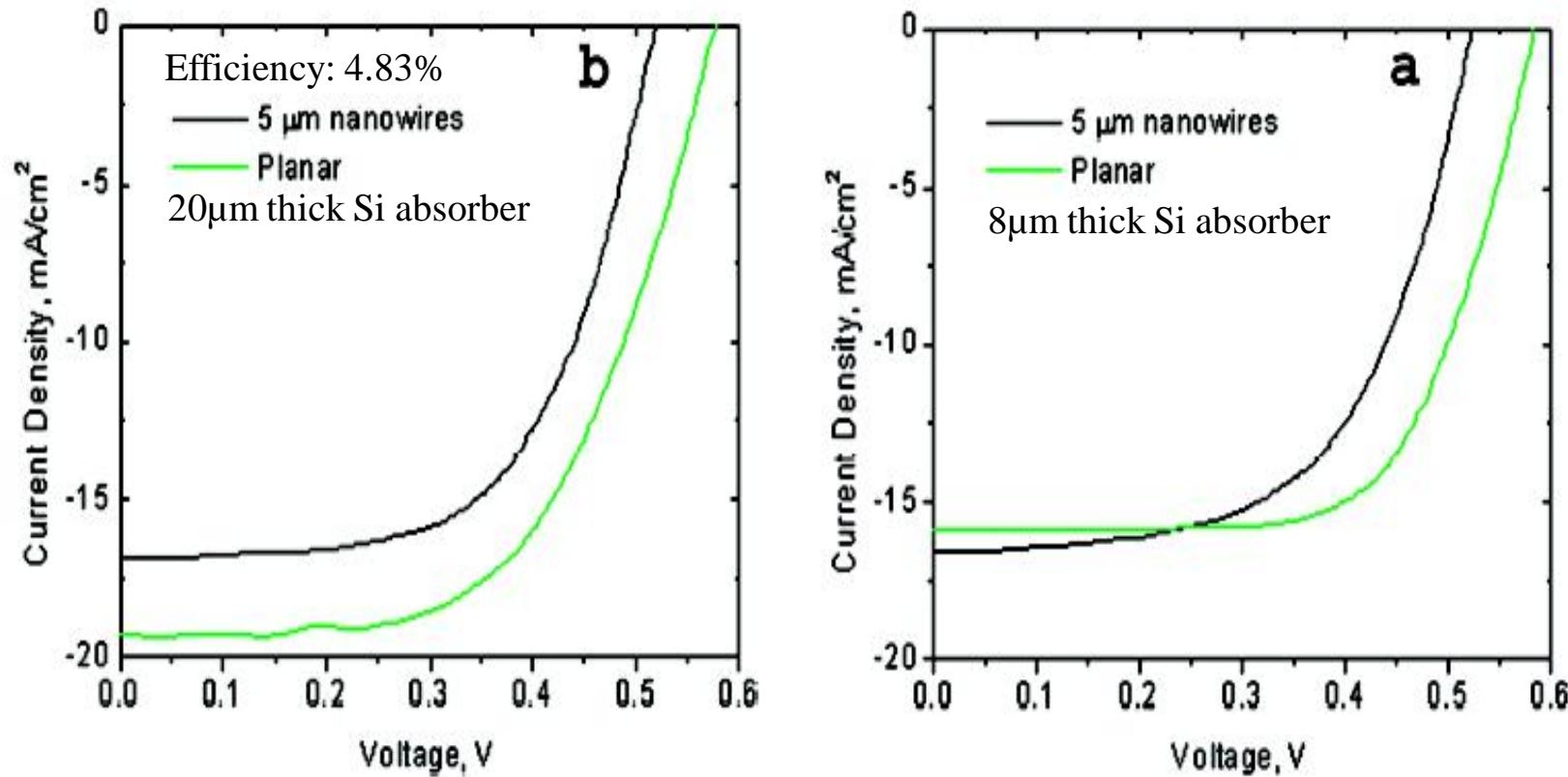
Guobin Jia, Martin Steglich, Ingo Sill, and Fritz Falk (IPHT),
2011





Towards miniaturisation

robust performance against thin film solar cells
PV technology platform sets poly-Si thickness <100 μm in 2030

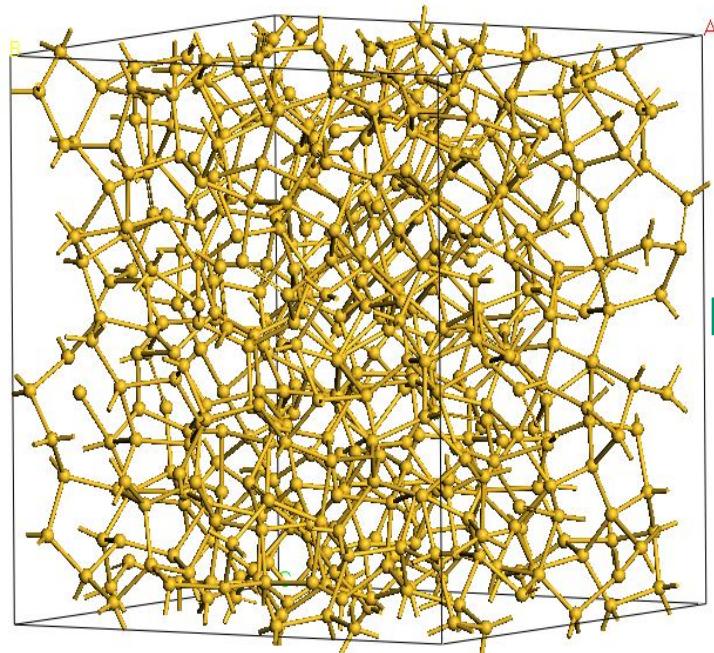


Erik Garnett and Peidong Yang, Nano Lett. **10**, 1082 (2010)

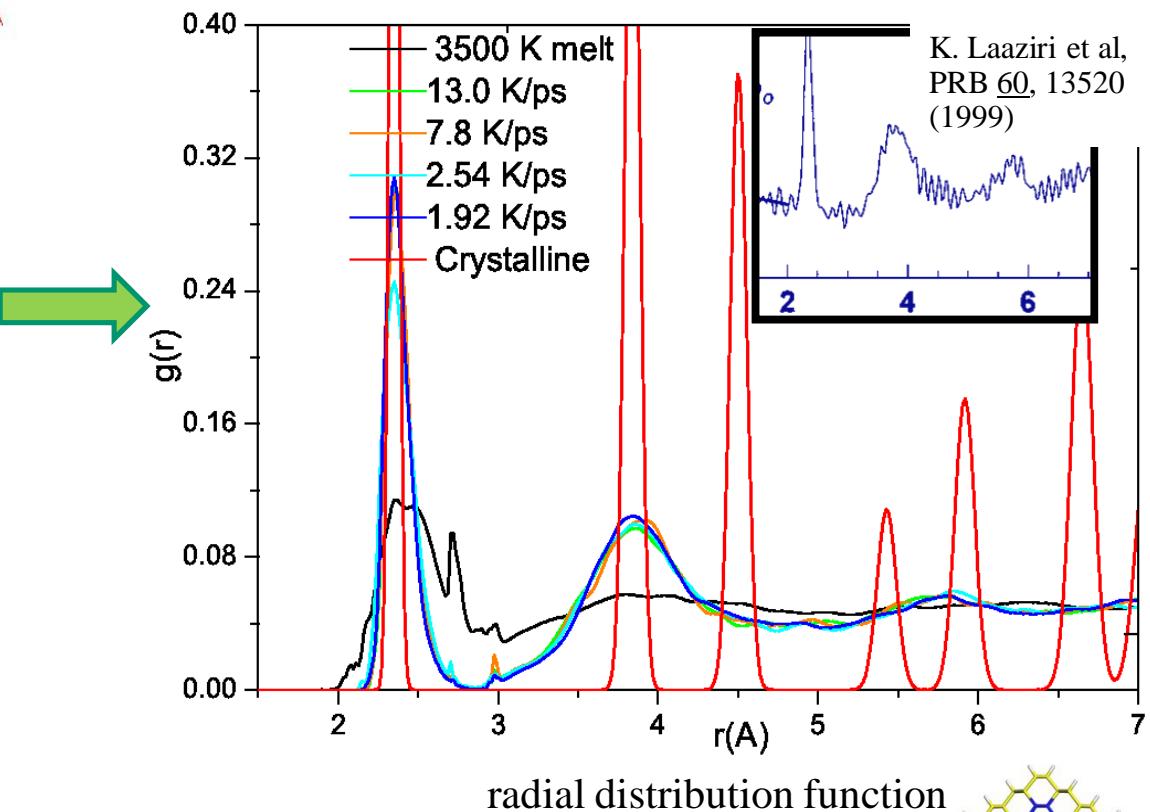


Atomic structure of a-Si (a-Si:H)

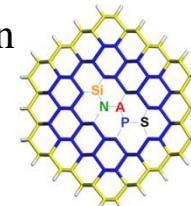
heat and quench MD method for structure generation



a-Si cell of 512 atoms
melt at 3500K – quench at 300K



radial distribution function

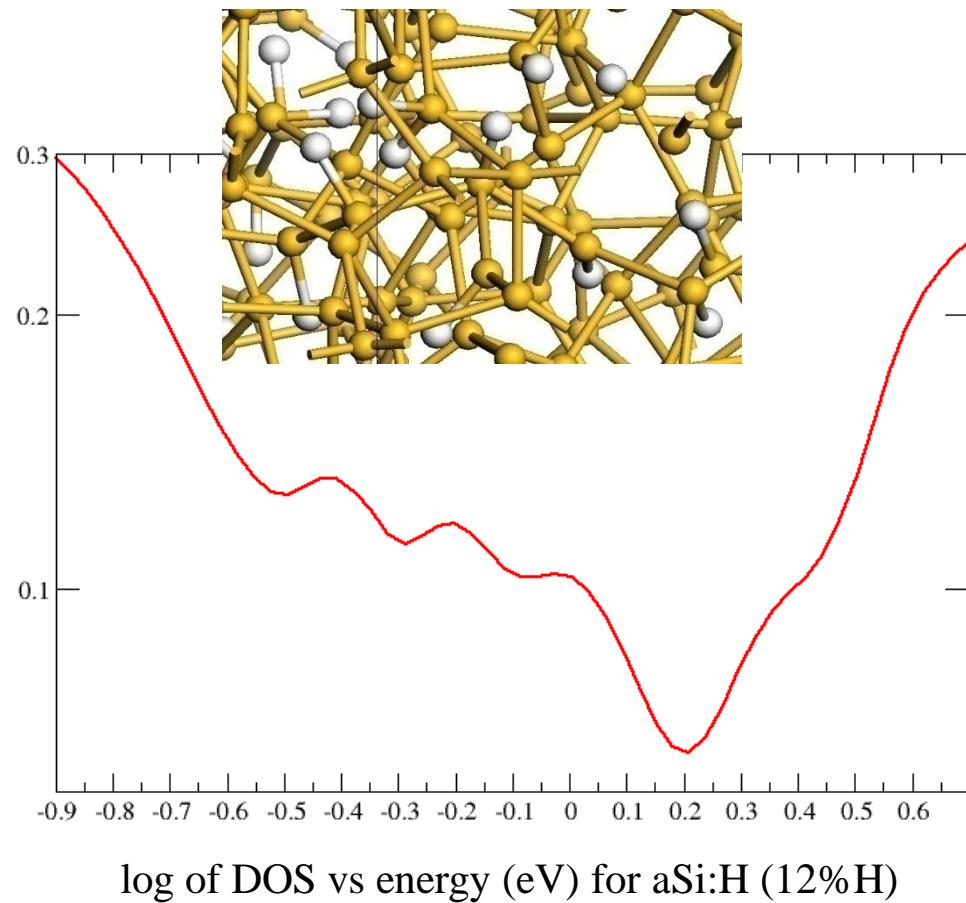


M. Legesse, M. Nolan and G. Fagas, unpublished



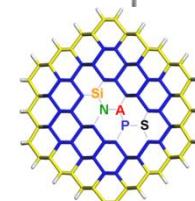
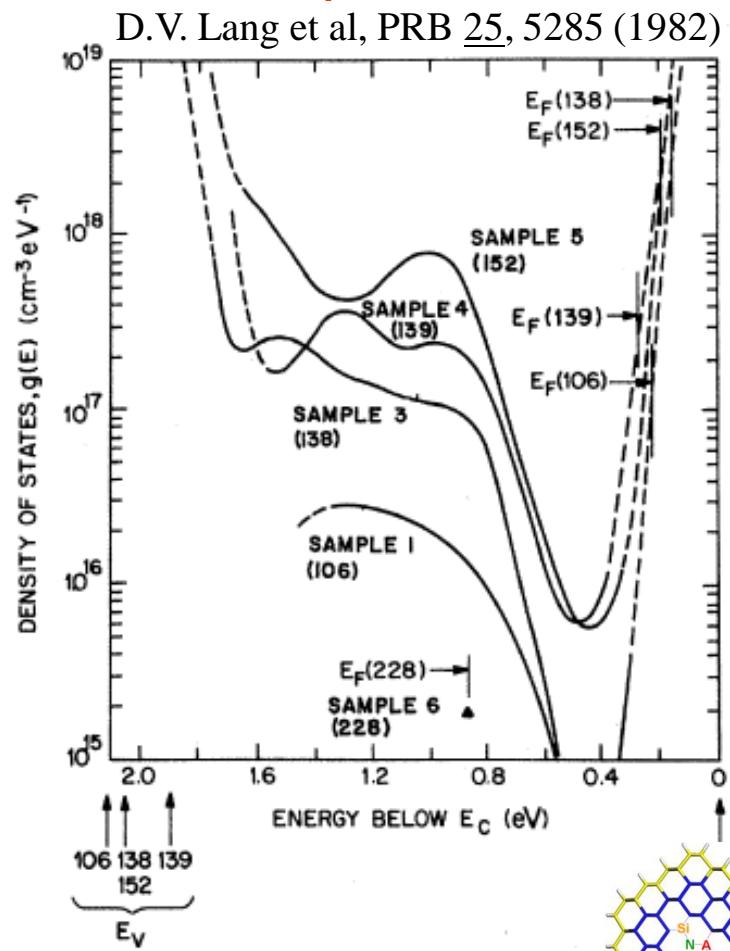
Electronic properties of hydrogenated a-Si

first-principles



M. Legesse, M. Nolan and G. Fagas, unpublished

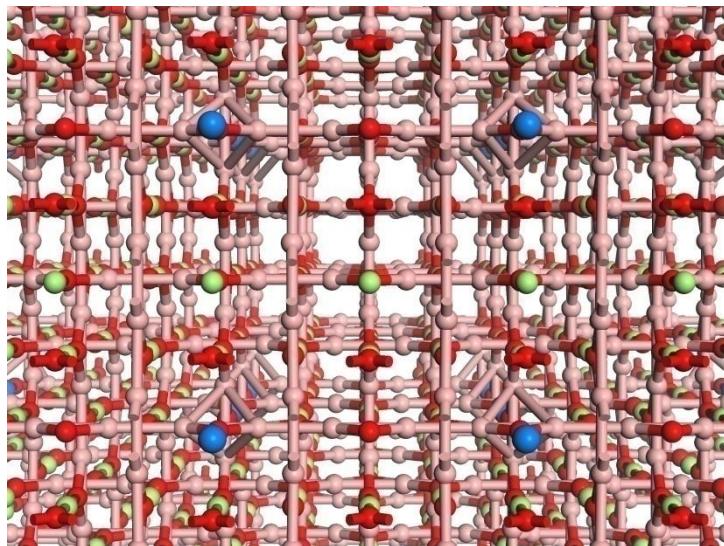
experiment



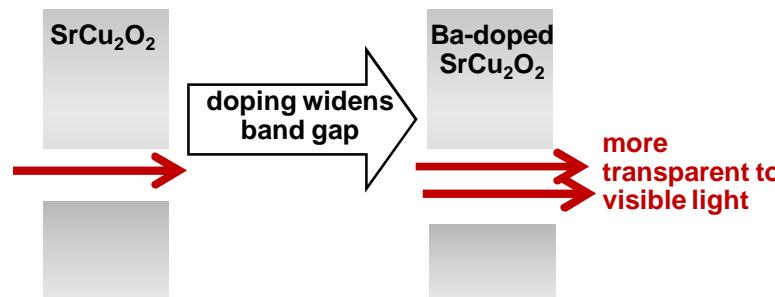


New materials for transparent electronics

CRYSTAL STRUCTURE OF Ba-doped SrCu_2O_2 ; blue=Ba, green=Sr, pink=Cu, red=O.



Ba distorts the structure, reducing Cu-Cu interactions and increasing the transparency to visible light. By contrast, other dopants reduce the transparency.



SCHEMATIC ELECTRONIC STRUCTURE showing gap between conduction band and Cu-derived valence band

Challenge: A p-type transparent conducting oxide (TCO) for transparent electronics.

Question Posed: Can we use modelling to design a new p-type TCO instead of traditional trial-and-error approach?

Results: Predicted a novel TCO, with optimal composition for transparency: Ba-doped SrCu_2O_2 .

Experiments by European partners confirmed its properties.

Material was licensed to Umicore and patented.

M. Nolan & S. D. Elliott, *Chem. Mater.* 20, 5522 (2008)

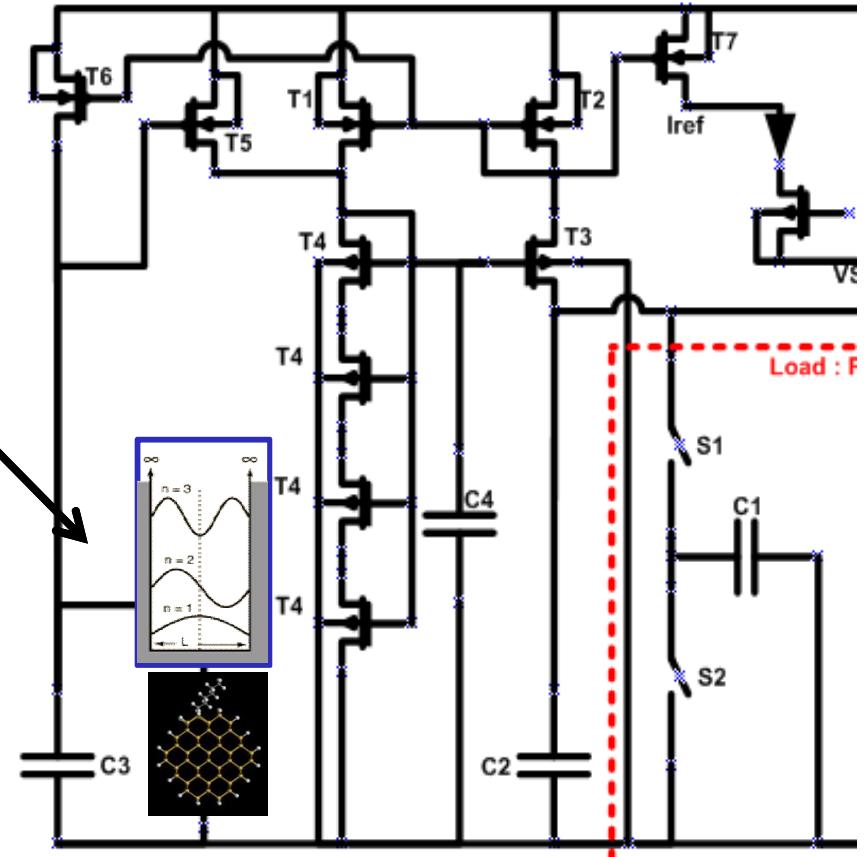
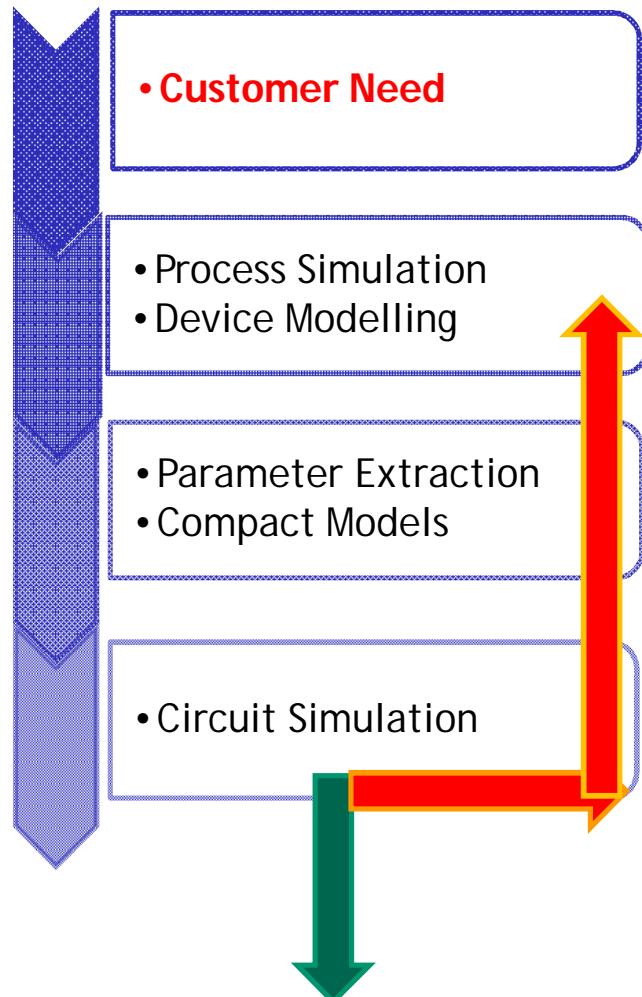


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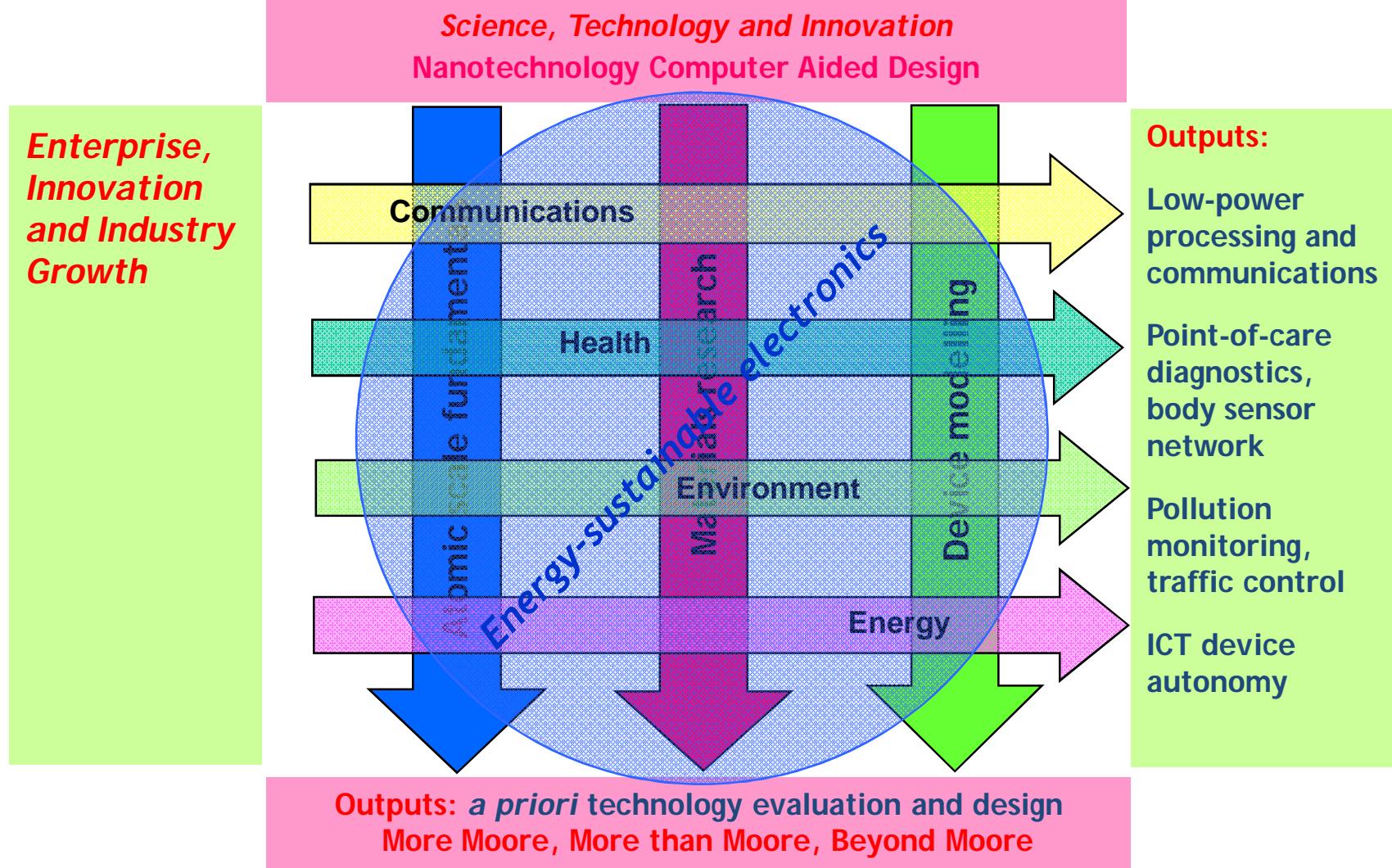
A modelling hierarchy for nano-inspired bottom-up technology design



30%-40% cost reduction



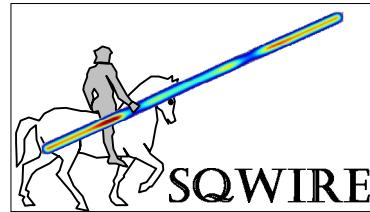
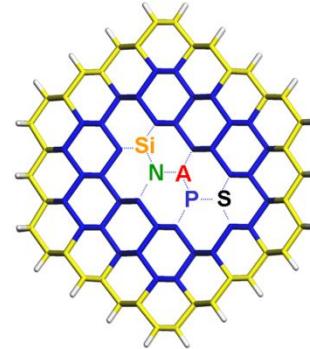
Impact of nanotechnology designed for ICT





Acknowledgments

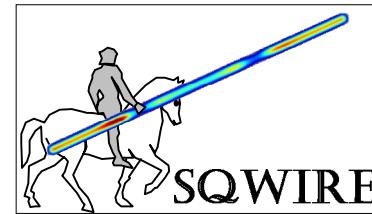
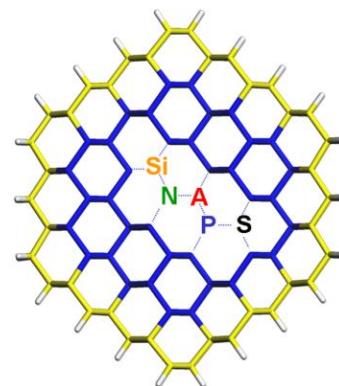
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Prof Fritz Falk (IPHT)
Dr Baruch Feldman (Weizmann Institute)
Prof Jim Greer (Tyndall, ETG director)
Marios Iakovidis (Tyndall, ETG)
Merid Legesse (Tyndall, ETG)
Dr Philip Murphy-Armando (Tyndall, CMT group)
Dr Michael Nolan (Tyndall, ETG)
Pedram Razavi (Tyndall, USD group)
Dr Sadasivan Shankar (INTEL Santa Clara, Materials Modeling group)





Thank you!

Q&A



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