Memristor Based Circuits With Learning Capabilities

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J-O. Klein et al, Institut d'Electronique Fondamentale (IEF), Orsay, France
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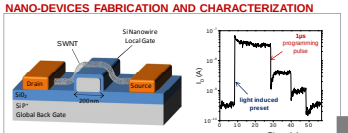
Nano-scale non-volatile memory devices present a number of potential advantages which include small size, low power and original functionality. Yet, they will prove useful only if the technological variability inherent to their scale can be handled. With their intrinsic tolerance to defects and auto-compensation capabilities, neuromorphic architectures allow lifting this roadblock. Nano-memristors, which are non-volatile programmable resistors, are ideally suited to be used as synapses in such architectures. We aim at studying a new class of scaled-down organic memory devices, building arrays of such devices, interfacing these memory blocks with CMOS electronics, proposing the associated learning algorithms and implementing such architectures.

Example of a completed project: Carbon-nanotube circuits with learning capabilities

ANR PANINI Project — NABAB Project

NANO-DEVICES FABRICATION AND CHARACTERIZATION

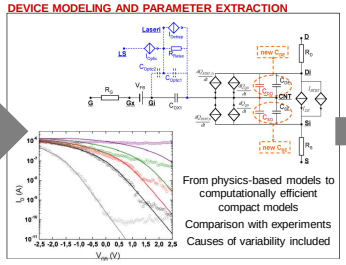


Device physics-based study of new type of nano-devices: in this example, carbon nanotube transistors are made light sensitive by a chemical coating and acquire non-volatile memory capabilities

Advanced Materials **18**, 2535 (2006)
Nano Letters **8**, 3619 (2008)
Small **6**, 2659 (2010)

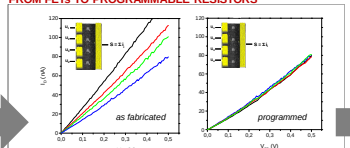
In collab. with D. Vuillaume at

DEVICE MODELING AND PARAMETER EXTRACTION



From physics-based models to computationally efficient compact models
Comparison with experiments
Causes of variability included

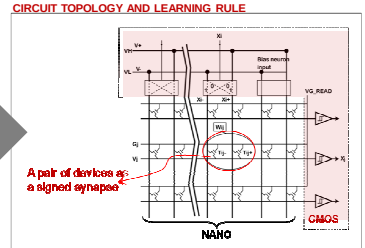
FROM FETs TO PROGRAMMABLE RESISTORS



Carbon Nanotube devices can be used as 2-terminal devices
Such use as programmable resistors allows compensating for devices to devices variability at the programming or learning step

Advanced Materials **22**, 702 (2010)

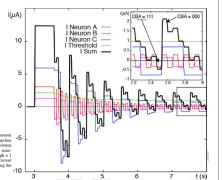
CIRCUIT TOPOLOGY AND LEARNING RULE



Based on the device characteristics, a circuit topology of a neural circuit and a specific learning rule are proposed

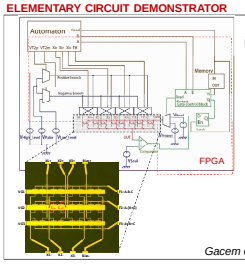
Synapses are based on nanodevices, neurons are implemented in conventional CMOS

Device modeling and circuit simulations are used to evaluate the capabilities of such mixed circuit to learn Boolean functions

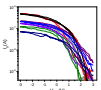


IEEE Trans. on Circ. and Syst. (2011)

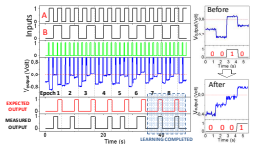
ELEMENTARY CIRCUIT DEMONSTRATOR



Micro-fabricated nanotube devices (with significant variability) are interfaced with conventional electronics. An FPGA emulates the CMOS part (learning rule, signal processing).

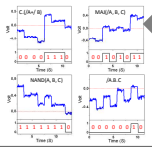


Gacem et al, in preparation



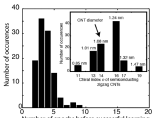
First example of a mixed circuit integrating nano-objects (here carbon nanotubes) that can acquire its function in a post fabrication learning step

Result of the learning of different 3-input logic functions



IMPACT OF TECHNOLOGICAL VARIABILITY

Through modeling, the impact of the technological variability on the efficiency of the function learning can be assessed. In this example, the variability on CNT diameter only impacts the number of learning cycles before successful learning



While successful, this project shows the limits of 3-terminal memory-devices and lead us to consider preferentially 2-terminal devices in particular Memristors

Memristors as synapses

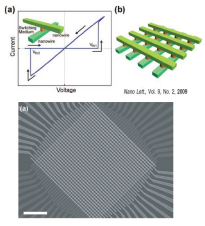
2-terminal non-volatile memory devices are one member of the large family of ***Memristive devices***. The activity devoted to Memristors (and resistive memory devices in general) has increased significantly since 2008 in particular (but not only !) through the contributions of the HP Labs.

✓ Memristors are easy to integrate in regular crossbar structures

✓ Despite their simple topology and small footprint, they show a high level of functionality

✓ Non-volatile memristors can be implemented in various technologies: oxides, phase-change materials, spintronics, molecular electronics, organic electronics, electrochemical conductive-bridge technologies etc.

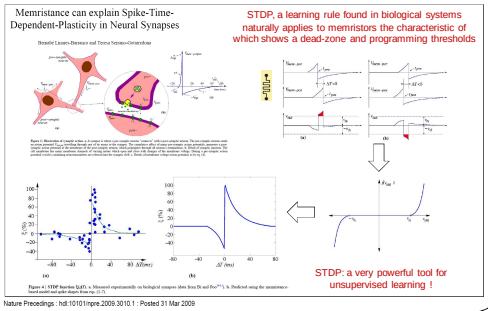
× Nanoscale memristors suffer from device-to-device variability: **need for new architectures such as programmable or neuromorphic architectures (in which memristors are used as synapses in combination with CMOS neurons)**



Example from U. of Michigan

Memristance can explain Spike-Time-Dependent-Plasticity in Neural Synapses

STDP, a learning rule found in biological systems naturally applies to memristors the characteristic of which shows a dead-zone and programming thresholds

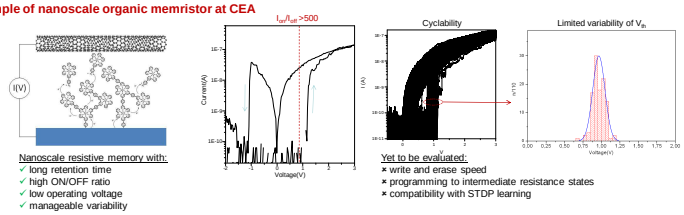


STDP: a very powerful tool for unsupervised learning !

Nature Precedings : hdl:10101npre.2009.3010.1 : Posted 31 Mar 2009

Toward memristor based circuits with learning capabilities

Example of nanoscale organic memristor at CEA

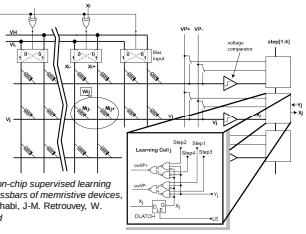


Nanoscale resistive memory with:
✓ long retention time
✓ high ON/OFF ratio
✓ low operating voltage
✓ manageable variability

Yet to be evaluated:
× write and erase speed
× programming to intermediate resistance states
× compatibility with STDP learning

The same methodology as for nanotubes can be applied to nano-scale organic memristors (device fabrication and characterization, compact modeling, circuit topology and learning rule proposal, circuit simulation, demonstrator fabrication and evaluation)

Example of Memristor-based architecture at IEF



Low overhead on-chip supervised learning methods for crossbars of memristive devices. J-O. Klein, D. Chabi, J-M. Retrouvey, W. Zhao, *submitted*

Challenges and prospects for green-ICT

► Can the combination of nano-scale non-volatile memristors and conventional CMOS achieve complex functions with lower energy consumption than CMOS alone?

► Can the co-integration of heterogeneous technologies be achieved without performance degradation?

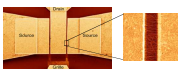
► Energy and addressing issues in 3D stacks of memristors?

►To what extend can adaptive / neuromorphic architectures compensate for device variability at the nanoscale?

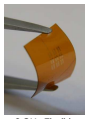
Molecular Electronics Lab. (LEM) IRAMIS Institute, CEA-Saclay

Vincent Derycke, Stéphane Campidelli, Pascale Chenevier, Arianna Filoramo, T. David (techn.), 3 Ph.D. students and 3 postdocs

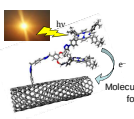
Carbon nanotube memory devices
Carbon nanotube HF Electronics
Graphene Electronics
Molecular Electronics
Organic Devices
Memristors & nano-memristors
Chemistry and bio-chemistry for nanosciences



80 GHz Nanotube-FETs (coll. IEMN)



2 GHz Flexible Graphene FETs



Molecules-CNT assembly for photovoltaic

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Nano-electronics Group COFI Department, IMS Bordeaux

Sébastien Frégonèse, Cristell Maneux, Thomas Zimmer
Ph.D. students and postdocs

The IMS MODEL team has a 15 years experience in device modeling. The two aspects: advanced device research and industrial applications are driven in parallel.

The compact modeling and device characterization activities are one of the two pillars of the ST-IXL joint-laboratory founded in 2003. Since 2005, the activities of the team move towards advanced nanoscale devices and especially to Carbon Nanotube Field Effect Transistor (CNTFET). First, within a French research program ACI "NANOSYS" 2007-2009, the IMS MODEL team has started to develop a CNTFET compact model. Within the French research programs PNANO "ACCENT" 2007-2010, Architecture du future "PANINI" 2008-2011 and ARPEGE "NANOGRAIN" 2009-2012, the MODEL team pursuits the development of the CNTFET's compact model including additional refinements: Schottky barrier contacts, tunneling effects, phonon scattering, multiple gates, light-induced effects, memory cells based on CNTFETs etc.

The team is also involved in compact modeling of graphene based devices.

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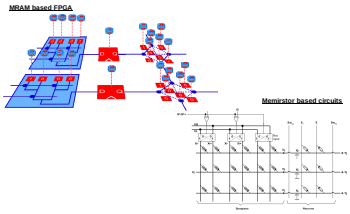
Architecture for Nanoelectronics NST Department, IEF Orsay

Jacques-Olivier Klein, Weisheng Zhao, Damien Querlioz, Yahya Lakys, (Post-Doc), Djaafar Chabi (PhD Student), Claude Chappert

The Nanoarchi Team designs integrated circuits (IC) and system-on-chip (SoC) architectures dedicated to emerging nanodevices. We focuse more specifically on two topics: magnetic nanocomponents applications (magnetic tunnel junction based MRAM, domain wall logic circuits) and new paradigms for computing and their applications to very high density post-CMOS nanocomponent assembly.



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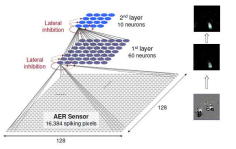
Nanocomputing Research Group LIST, CEA-Saclay

Olivier Bichler, Damien Querlioz, Christian Gamrat
Collaboration: Simon Thorpe

The group activity in neuromorphic hardware is rooted in early work on neurocomputers. With the advent of nanotechnologies, the group was one of the first in France to propose that such technologies be used for the design of neuromorphic hardware. The group has been very active at the European level by coordinating two major projects in the field of novel computing architectures: FP6-AETHER Integrated project and FP7-NABAB project on the development of architectures for nanofabricated synapse-like devices



Example: fully unsupervised learning of complex functions (pattern and trajectory recognition) based on arrays of (simulated) memristors used as synapses

O. Bichler et al, Int. Joint Conf Neur. Netw, (2011)
D. Querlioz et al, Int. Joint Conf. Neur. Netw. (2011)

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