Energy Efficient Application Specific Topology Generation for Network-on-Chip (NoC) Design

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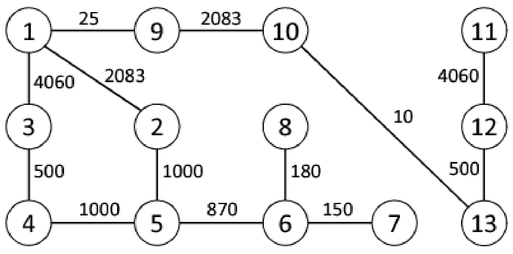
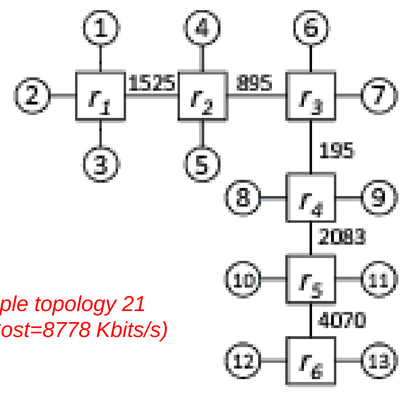
Introduction

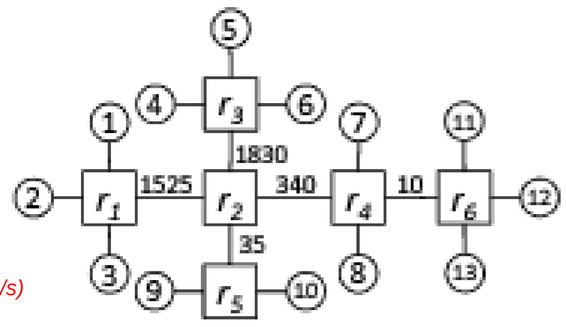
Network-on-Chip (NoC) is an alternative approach to traditional communication methods for System on Chip (SoC) architectures. Irregular topologies are preferable for the application specific NoC designs since they offer huge optimization space in contrast to their regular counterparts. Generating an application specific topology as part of the synthesis flow of a Network-on-Chip architecture is a challenging problem since there may be several topology alternatives, each of which may be superior to the others based on the different objective criteria. In this poster, we present a heuristic and a genetic algorithm based methods for this problem [3].



Core Flow Graph (CFG) of MP3 Decoder



An example topology 21 (CommCost=8778 Kbits/s)



An example topology 2 (CommCost=3740 Kbits/s)

Objectives

Energy model: The average energy consumption of sending one bit data from core v_i to core v_j can be calculated by

$$E_{T_{bit}}^{v_i,v_j} = \eta_{v_i,v_j} \times E_{S_{bit}} + \delta_{v_i,v_j} \times E_{L_{bit}}$$

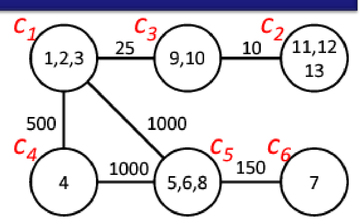
η_{v_i,v_j} : the number of routers the bit passes, δ_{v_i,v_j} : the length between source and dest. routers.

Problem: Given a CFG and a set of routers R with p ports, generate a topology T(R,L,F) such that, for every edge, there exists a routing path in T, router port bandwidth, link bandwidth, and chip area constraints are satisfied and the total energy consumption of the network (E_{NoC}) is minimized.

$$E_{NoC} = \sum_{\forall e_{i,j} \in E} w_{i,j} \times E_{T_{bit}}^{v_i,v_j}$$

TopGen: A Heuristic Method

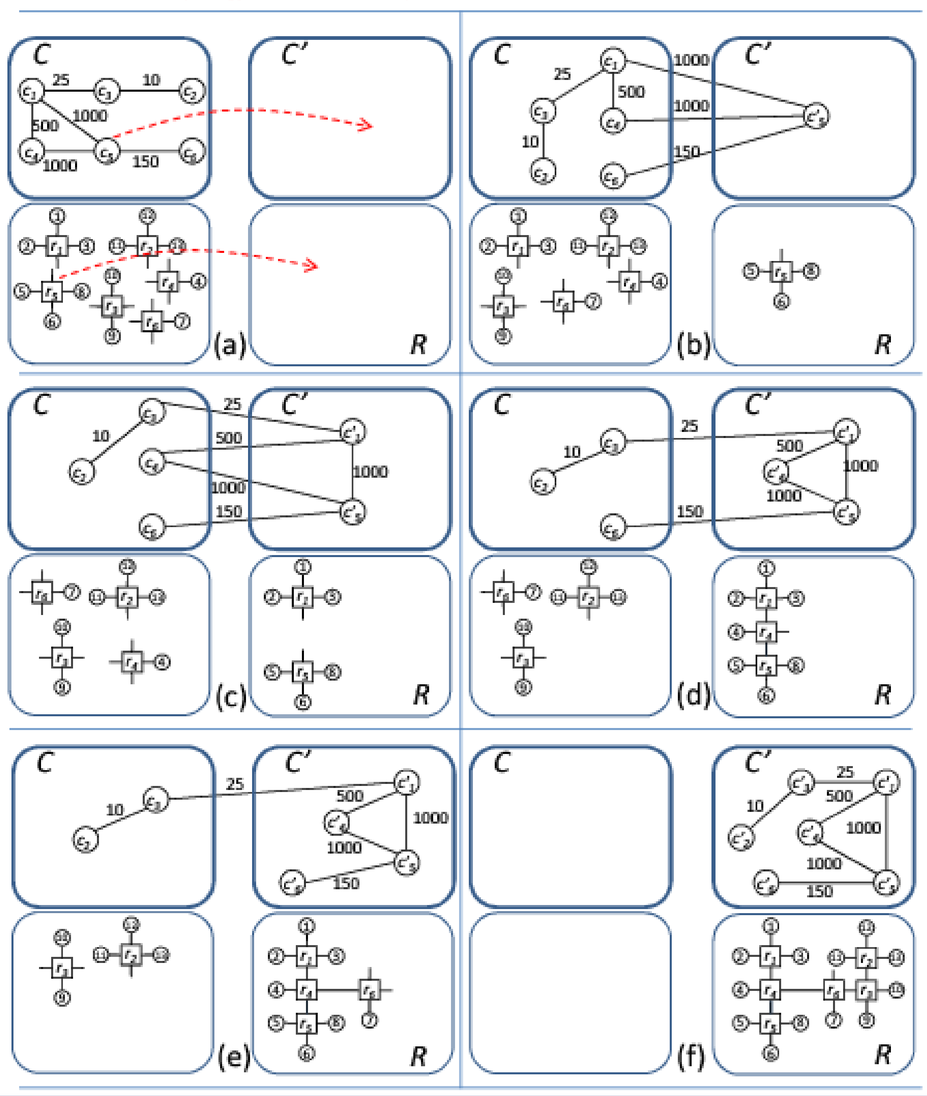
TopGen has two main phases: ***clustering and topology construction***. In the clustering phase, we decompose the given CTG into clusters based on the communication frequency of the cores. We simply try to place heavily communicating cores into the same cluster. Then, each cluster can be mapped to a router in the library.



Cluster Graph (CG) of MP3 Decoder

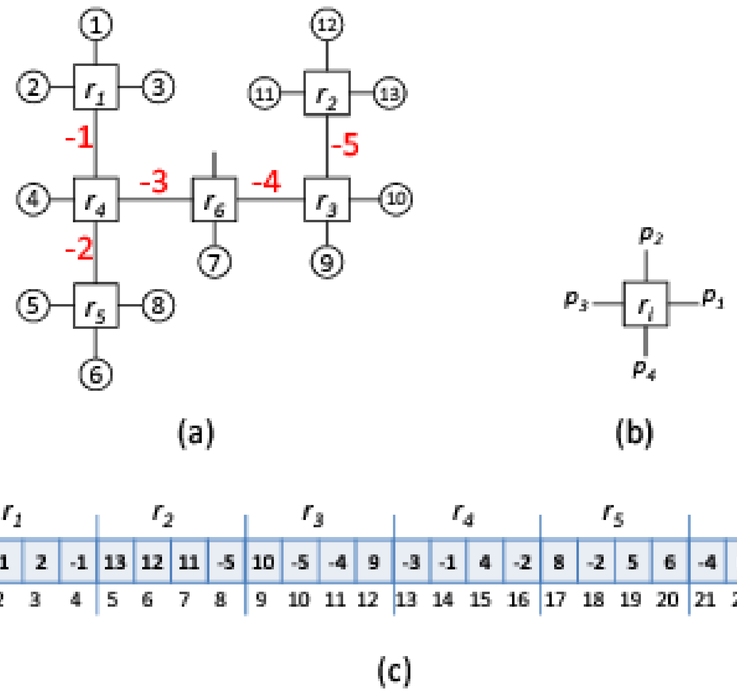
In topology construction phase, we iteratively connect routers to the network one by one, trying to connect heavily communicating routers as close as possible.

Topology construction step. Result -> CommCost=3885 Kbit/s



GATGA: A Genetic Algorithm based Method

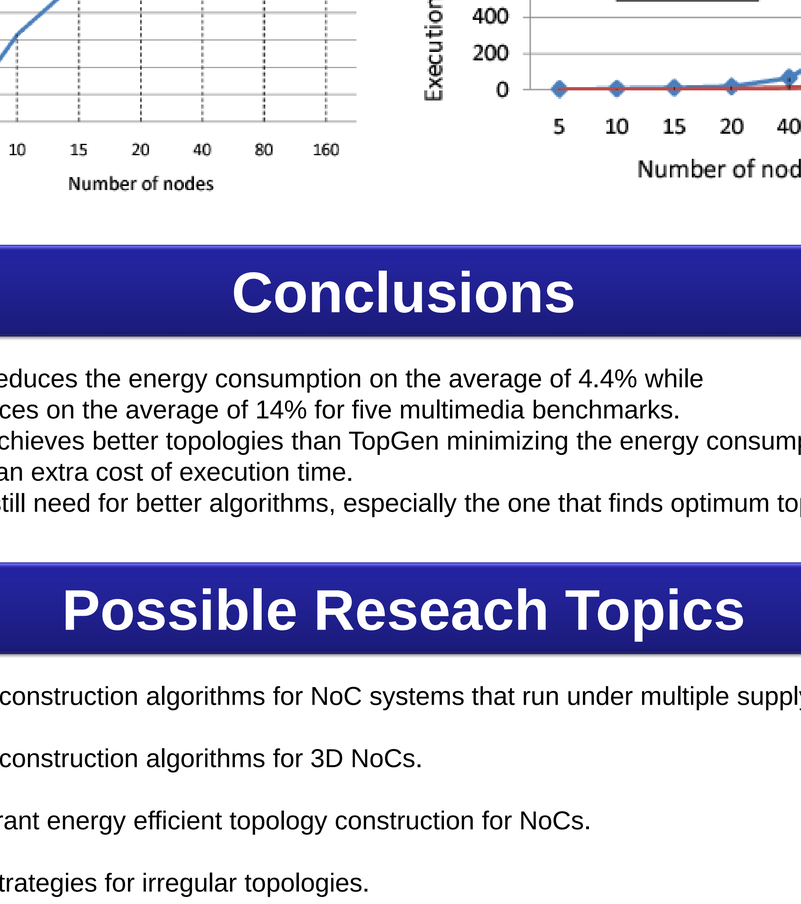
Genetic Algorithm based Topology Generation Algorithm (GATGA) is based on evolutionary computing. Each possible topology is represented as an individual string where router ports are the genes of the individual. GATGA is composed of 3 major steps, namely initialization, crossover, and mutation. It selects the fittest individual from the population of the solutions.



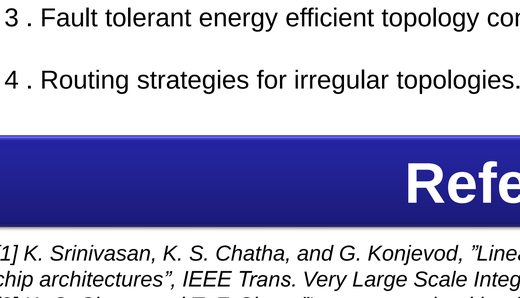
(a) A topology generated by TopGen. (b) Port labels of routers. (c) Chromosome representation of the given topology.

Results

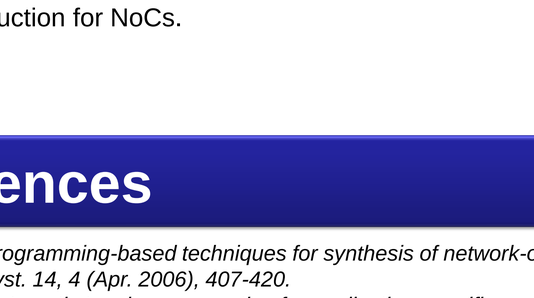
Energy consumption reduction of proposed methods against ILP [1] and PATC [2] algorithms on multimedia benchmarks.



Energy improvement of GATGA againts TopGen.



CPU time of GATGA againts TopGen.



Conclusions

1 . TopGen reduces the energy consumption on the average of 4.4% while GATGA reduces on the average of 14% for five multimedia benchmarks.
2 . GATGA achieves better topologies than TopGen minimizing the energy consumption of the system with an extra cost of execution time.
3 . There is still need for better algorithms, especially the one that finds optimum topologies.

Possible Reseach Topics

1 . Topology construction algorithms for NoC systems that run under multiple supply voltages.

2 . Topology construction algorithms for 3D NoCs.

3 . Fault tolerant energy efficient topology construction for NoCs.

4 . Routing strategies for irregular topologies.

References

[1] K. Srinivasan, K. S. Chatha, and G. Konjevod, "Linear-programming-based techniques for synthesis of network-on-chip architectures", IEEE Trans. Very Large Scale Integr. Syst. 14, 4 (Apr. 2006), 407-420.
[2] K.-C. Chang and T.-F. Chen, "Low-power algorithm for automatic topology generation for application-specific networks on chips," IET Comput. Digit. Tech., 2008, vol. 2, no. 3, pp. 239-249.
[3] S. Tosun, Y. Ar, and S. Ozdemir, "Application Specic Topology Generation Algorithms for NoC Design,", submitted to IET Comput. Digit. Tech.