Nanofabrics For Reconfigurable Computing Cores

P.E. Gaillardon, K. Jabeur, S. Le Beux, I. O'Connor, N. Yakymets ian.oconnor@ec-lyon.fr

inl.cnrs.fr

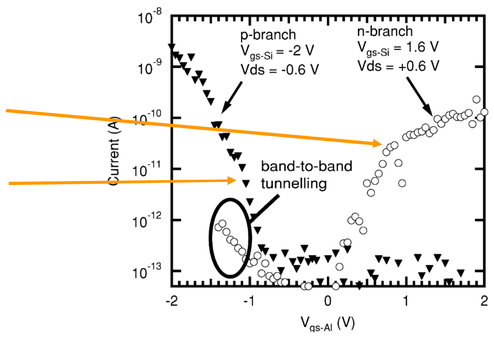
Context and objectives

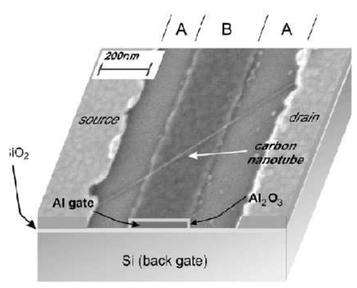
- Reconfigurable computing is a promising paradigm able to fill the gap between hardware and software by providing both flexibility and performance
- The emergence of novel nanodevices enable exploration of improvements on the performance envelope of reconfigurable logic circuits
- Goals:
  - Exploit specific properties of DG-CNTFETS (ambivalence) to create logic cells that can be configured by the transistor back-gates
  - Explore ways of associating logic cells for robust, flexible, high-performance nanofabrics

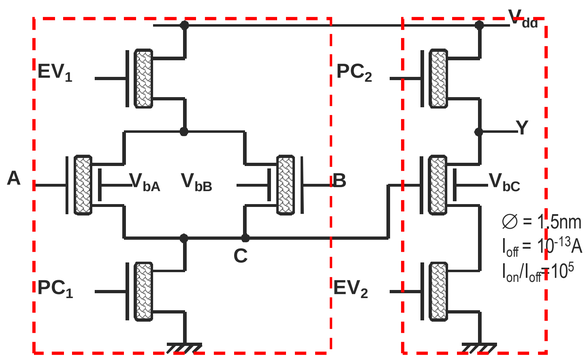
DG CNTFET dynamic-logic cells

- CNT_DRC_7T
  - Dynamically reconfigurable 2-input 14-function logic cell
  - 2 stages: logic function + follower/inverter (7T)
  - boolean data inputs A, B and output Y (logic levels at V_{ss}=0V and V_{dd}=+1V)
  - 3 control signals VbgA, VbgB, VbgC
  - four-phase non-overlapping clock signals

V_{fg}	V_{bg}	state
+V	+V	on (n)
-V	+V	off (n)
+V	-V	off (p)
-V	-V	on (p)
X	0	off (n/p)







J. Liu, I. O'Connor, D. Navarro, F. Gaffiot, *El. Lett.*, 43(9), April 2007

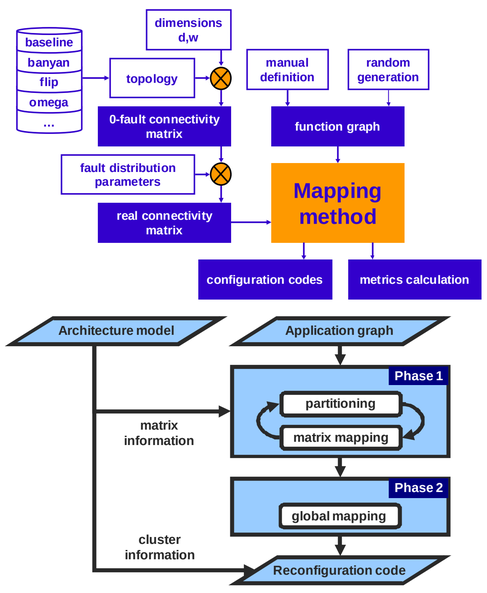
V_{bgA}	V_{bgB}	V_{bgC}	Y
+V	+V	+V	$\overline{A+B}$
+V	+V	-V	A+B
+V	-V	+V	$\overline{A.B}$
+V	-V	-V	$A+\overline{B}$
-V	+V	+V	$A.\overline{B}$
-V	+V	-V	$\overline{A+B}$
-V	-V	+V	A.B
-V	-V	-V	$\overline{A.B}$
+V	0	+V	$\overline{A}$
+V	0	-V	A
0	+V	+V	$\overline{B}$
0	+V	-V	B
0	0	0	1
0	0	-V	0

Parameterized model of cell cluster

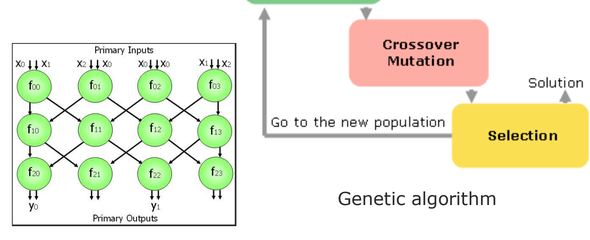
- Integration density and switchbox overheads lead to exploration of fixed interconnect topologies between logic cells organized into clusters
- Parameters: cluster width and depth, interconnect topology
- Tradeoffs between
  - number of realizable functions, overall functionality
  - level of reconfigurability of the cluster size and interconnect topology

Function mapping methods

- Hybrid branch-and-bound / genetic algorithms
- Initial data: architecture (cluster width and depth), interconnect topology, truth table or function graph
- Tradeoffs between: mapping success rate, cluster size, diversity of realizable functions

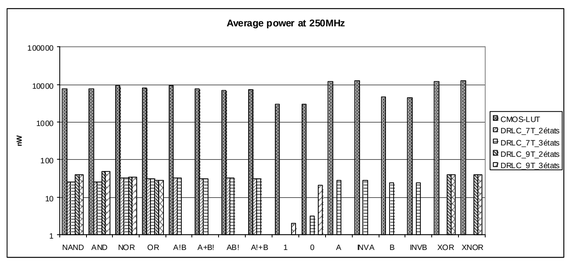


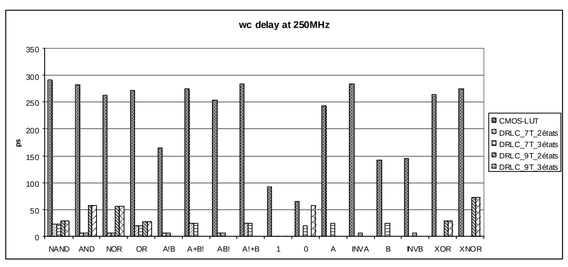

```
Set a Cluster_Size
Set an Interconnect_Topology
While (i <= Max_Number_of_Outputs)
  While (j <= Max_Number_of_Inputs)
    While ( k <= Number_of_Truth_Tables)
      Generate a Truth_Table(i, j)
      Run GA up to N populations
      Increment k
  Increment j
Increment i
```

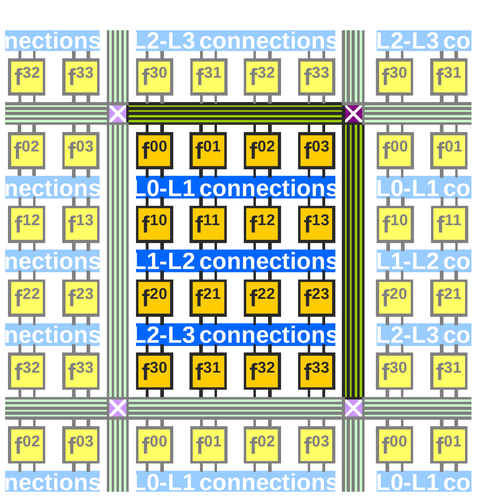


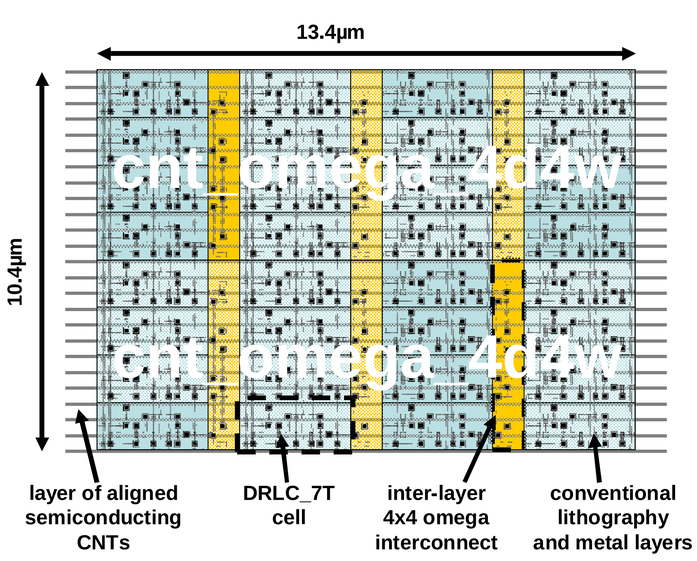
Results and achievements

- Back gate DG-CNTFET reconfigurable dynamic-logic cells
- Cadence (Spectre) simulations shows max. gain of 90% in terms of latency and power consumption compared to LUTs in CMOS 65 nm technology



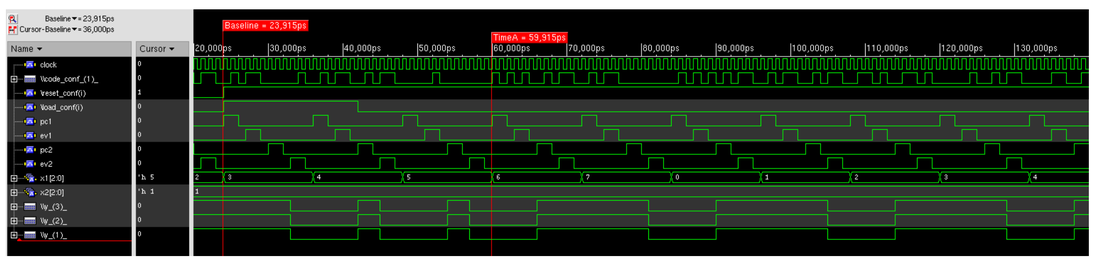




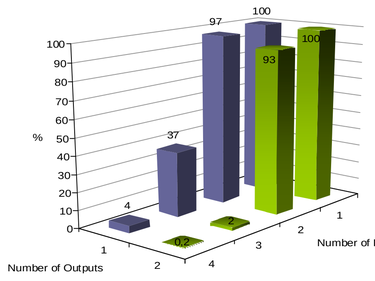


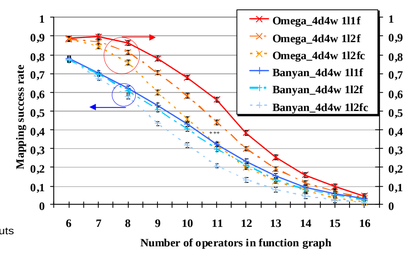
Results and achievements

- Parameterized model is implemented using SystemC
- Function mapping method is implemented in Matlab



Mapping success rate for a cluster of 2×2 cells, %





Mapping success rates for Banyan and Omega interconnect topologies within a 4×4 cluster in presence of faults

Benchmk circuit	No. operations	No. depend-encies	Logical depth	No. sub-fonctions	No. depend-encies	Fill factor	No. hw placement failures
ALU2	45	64	14	6	9	7.5	1
CMP8	59	75	11	9	14	6.5	2
ADD8	101	132	22	11	18	9.18	0
ADSU8	133	180	25	18	30	7.33	0
CMP16	142	189	22	19	41	7.47	2
ADD16	197	260	38	21	36	9.38	0
ADSU16	261	356	41	27	49	9.68	1

Funding and support

- ACI Nanosys
- ANR-PNANO Multigrilles, ANR-ARPEGE NANOGRAIN

Main partners and collaborations

- CEA-LETI / DACLE (FR), IMS (FR)
- Ecole Polytechnique de Montréal (CA), EPFL (CH)