Energy Modulated Computing

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EPSRC Pioneering research and skills

Newcastle University

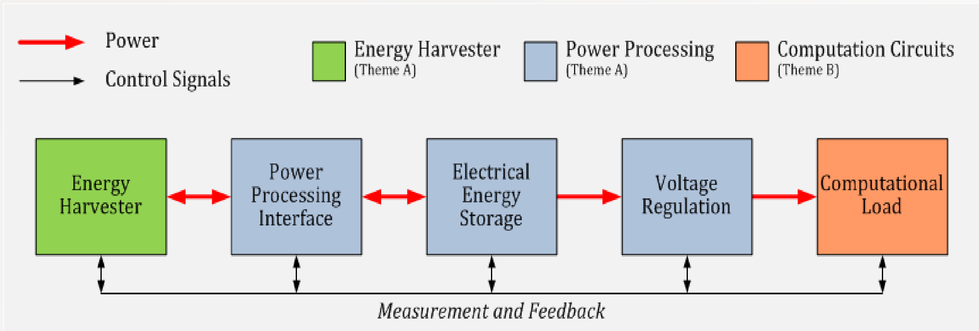
holistic energy harvesting

Abstract

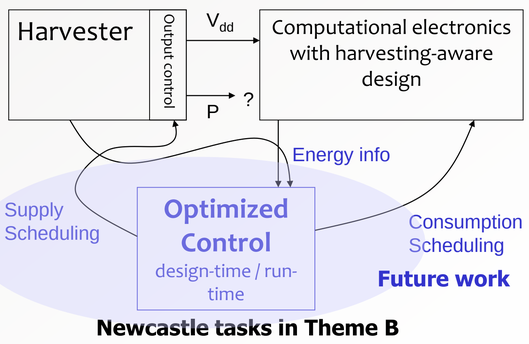
Increasingly, energy and power turn from optimization criteria into design constraints, sometimes as critical as, for example, reliability and timing. Furthermore, quanta of energy or specific levels of power can shape the system's action. In this direction, **we propose to develop a systematic approach to designing computing systems that are energy-modulated and power-adaptive**. This will cover systems where power comes from energy harvesting sources with limited power density and/or unstable levels of power. Initial studies have been performed at Newcastle that include self-powered sensors, variation-resilient logic and memory operating in the dynamic range of Vdd 0.2-1V, and system design techniques for power-adaptation.

Next Generation Energy-Harvesting Electronics: Holistic Approach, Southampton, Newcastle, Imperial and Bristol: £1.6M EPSRC funding

We are entering the era of electronics powered by energy harvesters (EH). Future self-powered applications will require more complex and compact electronics that are also intelligent, adaptive and able to perform more computation with less energy. **Holistic** is dedicated to mixed-technology approach to research into **EH-powered systems**. A key factor for the computation load is **variable Vdd**.



Overall system vision



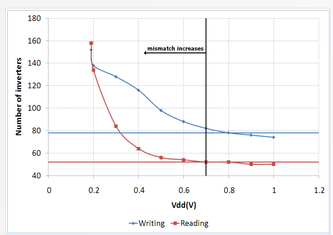
Newcastle tasks in Theme B

Energy Proportionality

- **Energy-harvesting** changes the dynamic balance between supply and consumption – supply add operational constraints in real-time
- **Adaptation to power changes** should be at all levels of abstraction, from logic cells to systems
- Asynchronous (self-timed) techniques support more effective adaptation to Vdd changes via natural temporal robustness; they also offer better energy proportionality
- Good energy characterisation of loads (logic, memory, i/o, RF) is essential for high-quality adaptation
- More theory, models and algorithms are needed for handling the problem of power-adaptation in run-time

Memory-logic delay mismatch

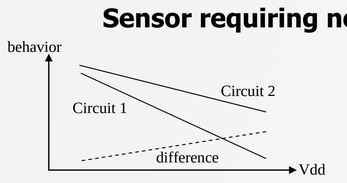
A fundamental discovery influencing both **voltage sensor** and **SRAM** designs

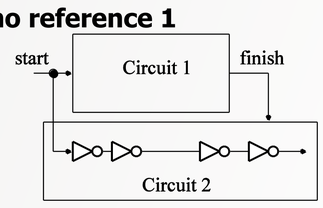


On-chip Reference free voltage sensing

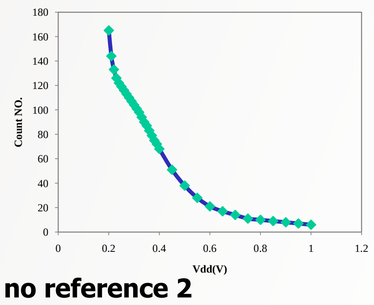
Supply voltages, which tend to be variable, are important parameters for EH-powered systems, esp. for optimization and control. **Voltage sensors** which can work under variable Vdd without or with minimal reference requirements are therefore indispensible elements.

Sensor requiring no reference 1

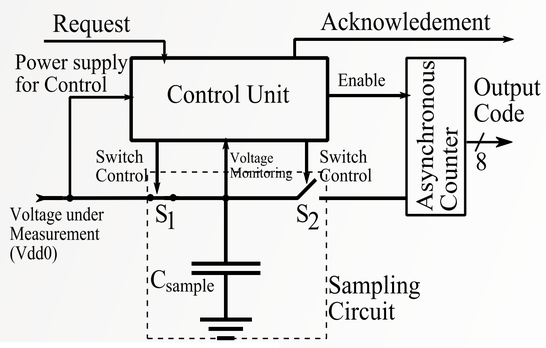


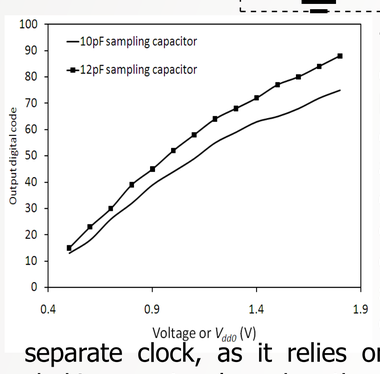


Taking advantage of the **Memory-logic delay mismatch** and using an SI SRAM cell as Circuit 1 and normal delay elements (chain of inverters) as Circuit 2, a fully reference-free voltage sensor has been built which has high voltage measurement precision and good performance.



Sensor requiring no reference 2



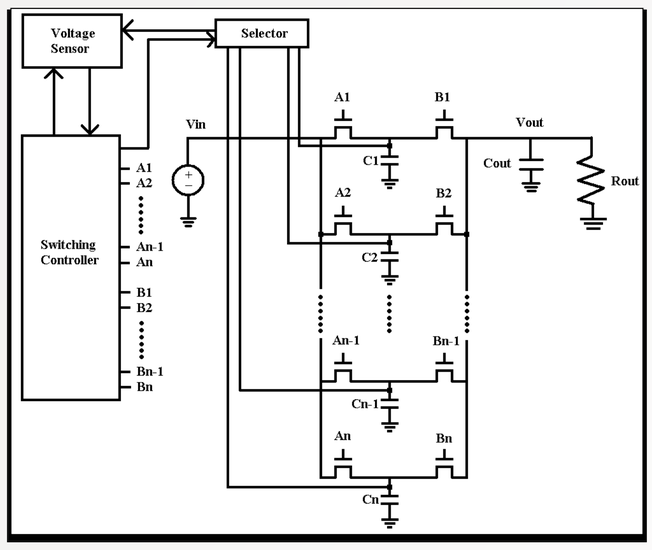


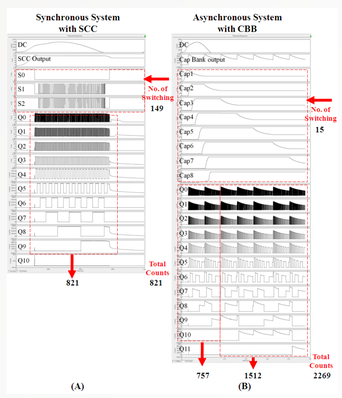
This voltage sensor consists of a capacitor-based sampling circuit, control unit and an asynchronous toggle counter circuit. The binary counter works using the charge stored in the sampling capacitor. This counter does not require a separate clock, as it relies on the asynchronous hand-shaking protocol under the principle of semimodular circuits. The key feature of this method is that the counter is entirely powered by the energy of the charge obtained from the voltage it measures, and the speed at which it works reflects this voltage. This makes the design energy-proportional.

Newcastle University's International Patent Application - PCT/GB2011/050390

On-chip energy storage and power control/delivery

Switched capacitor converters (SCC) were conventionally used as DC/DC converters to maintain Vdd delivered to computational electronics. Asynchronous computational electronics have been shown to tolerate a wide range of variance in Vdd. This has allowed the development of a novel on-chip energy storage and power control method using capacitor bank blocks (CBB) with superior efficiency.

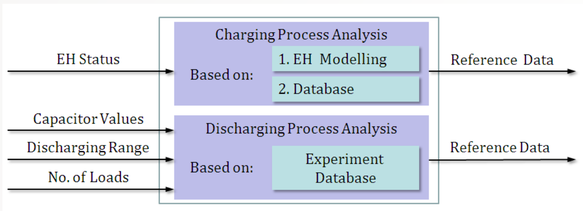




More computation for the same harvested energy with CBB.

Further studies including detailed characterization of example systems have been carried out.

- SCC is a **special case** of CBB
- CBB can provide a much higher degree of **programmability** in terms of **power and energy scheduling** (different capacitor values, different charging/discharging points, etc.)
- This leads to more **effective**, not just **efficient** energy usage by directly ensuring energy/power proportionality and modulating task execution with energy provisions
- CBB is especially suitable for systems where both data and energy inputs display strongly **aperiodic behaviours** – cf. SCC being fundamentally designed for steady or at least periodic operational regimes thus unsuitable for energy harvesting



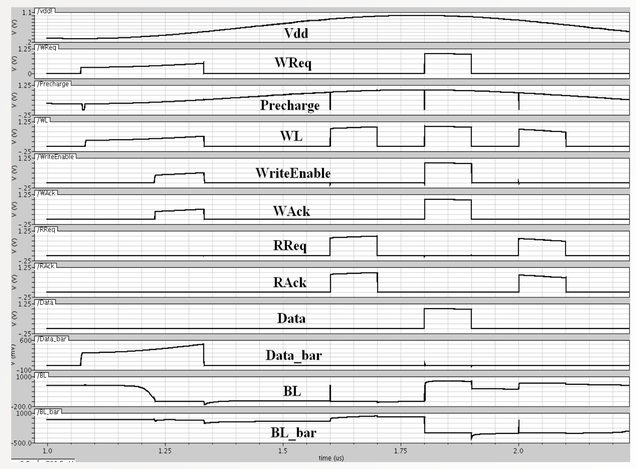
ASYNC 2011

ACM JETC

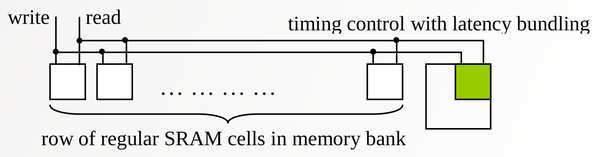
Memory subsystem working under variable Vdd

Non-deterministically variable Vdd is a characteristic of EH-powered systems. Computational electronics including memory subsystems must work under such an environmental assumption.

SRAM which can work under variable Vdd efficiently poses a number of challenges, best met with asynchronous technology. Full completion detection and acknowledgement for writing in SRAM was previously regarded as either impossible or impractical. In this project, we developed fully speed independent SRAM with completion detection for both reading and writing actions for the first time and demonstrated the efficiency of this method.



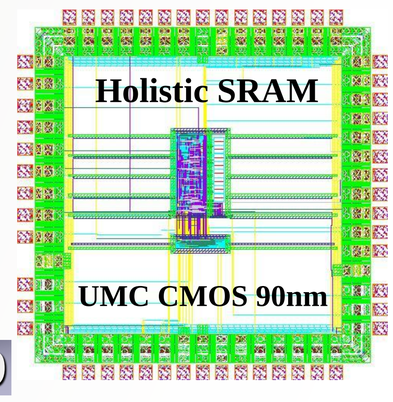
Working under variable Vdd



Time-bundled SRAM with fully SI cell as bundling unit

Bundled data SRAM

Bundled-data approach is an efficient way of designing asynchronous systems and memory is a natural bundling target. Owing to the **memory-logic delay mismatch**, bundling of memory cannot be done with conventional delay elements. We have used fully SI SRAM cells for bundling to overcome this difficulty.



PATMOS 2010

JOLPE

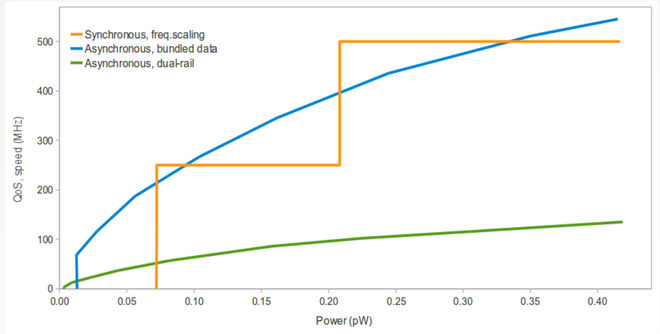
PATMOS 2011

Adjustable Quality of Service (QoS)

Computation time as the QoS

Several implementations of an 8-bit Booth's multiplier were analysed in Spectre analogue simulator. Their power consumption was characterised for a wide spectrum of supply voltages - it was reduced in small steps from a nominal value until the circuit started malfunctioning.

- Synchronous (rigid 1GHz clock)
- Frequency scaling (changeable 1GH, 500MHz, 250MHz clock)
- Asynchronous bundled data (extra control logic and delay lines)
- Asynchronous dual-rail (double comb. logic and register size, extra completion detection and single-rail to dual-rail converters, double switching activity)



Computation precision as the QoS

The following Fast Fourier Transform (FFT) benchmarks were simulated in Synopsys VCS at fixed supply voltage while changing the computation precision (transform size and data representation). The power consumption was estimated in Synopsys PrimeTime with PX extension.

- Non-reconfigurable implementation (fixed 1024 points transform size)
- Reconfigurable transform size (1024 / 512 / 256 points)
- Reconfigurable data precision (16 / 12 / 8 bits)
- Reconfigurable transform size and data precision
- Asynchronous bundled data implementation of fully reconfigurable FFT

All the benchmarks were synthesised for Faraday library based on UMC 90nm technology process.